The Liberty Simulation Environment ASPLOS XI Tutorial

Jason Blome
University of Michigan

Prof. Manish Vachharajani
University of Colorado

Neil Vachharajani, Prof. David August
The Liberty Research Group
Princeton University

The Liberty Simulation Environment (LSE)

LSE in One Slide

- LSE is not a simulator!
- LSE defines a HARDWARE DESCRIPTION LANGUAGE

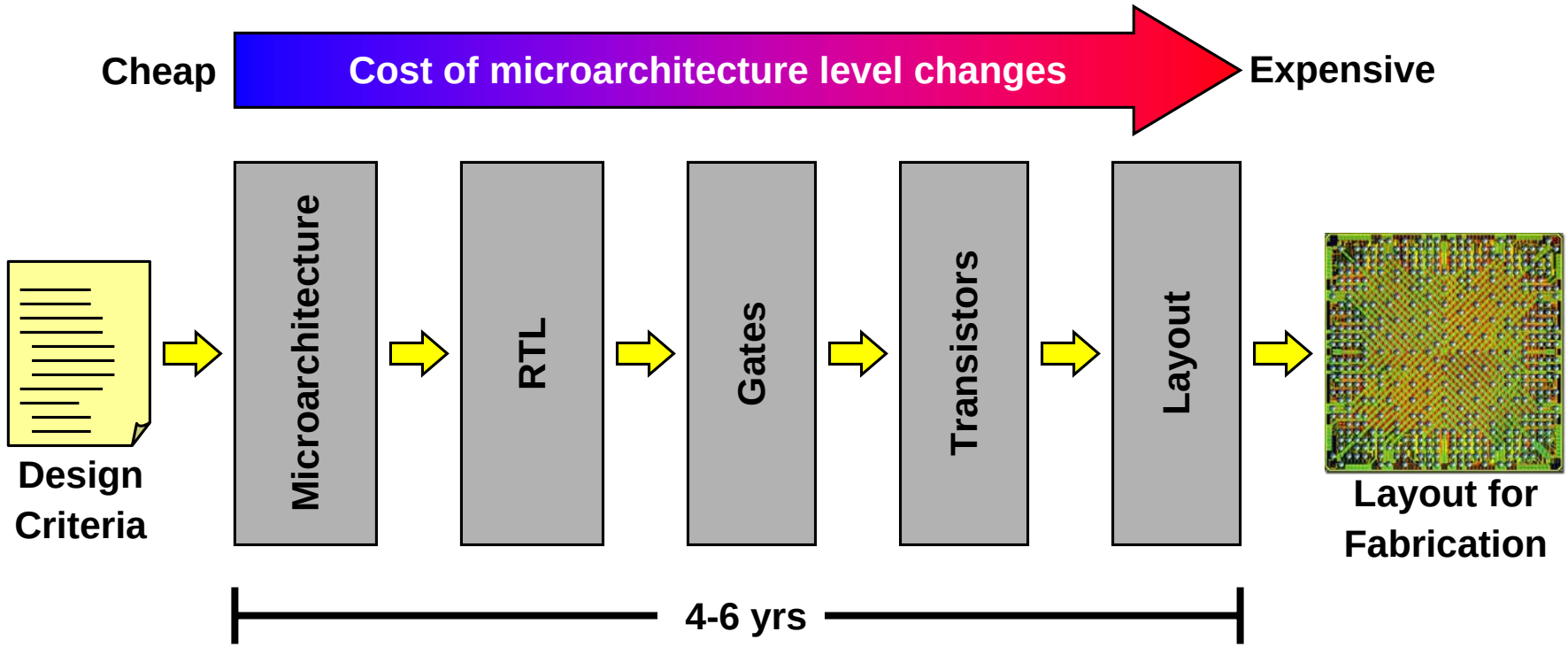
- LSE is a collection of TOOLS:
  - Simulator Builder
  - Visualizer
  - Others...

- LSE supports collections of COMPONENTS and DOMAINS:
  - The Core Library (arbiter, queue...)
  - Architecture Libraries (branch predictors, cache components...)
  - Instruction Set Emulators (IA-64, PowerPC, DLX, MIPS...)
  - Third Party Integrators (BLiSS:SimpleScalar, Simics...)
  - Domains (Checkpointing, Sampling, Clock, Emulator...)

Tutorial Sequence

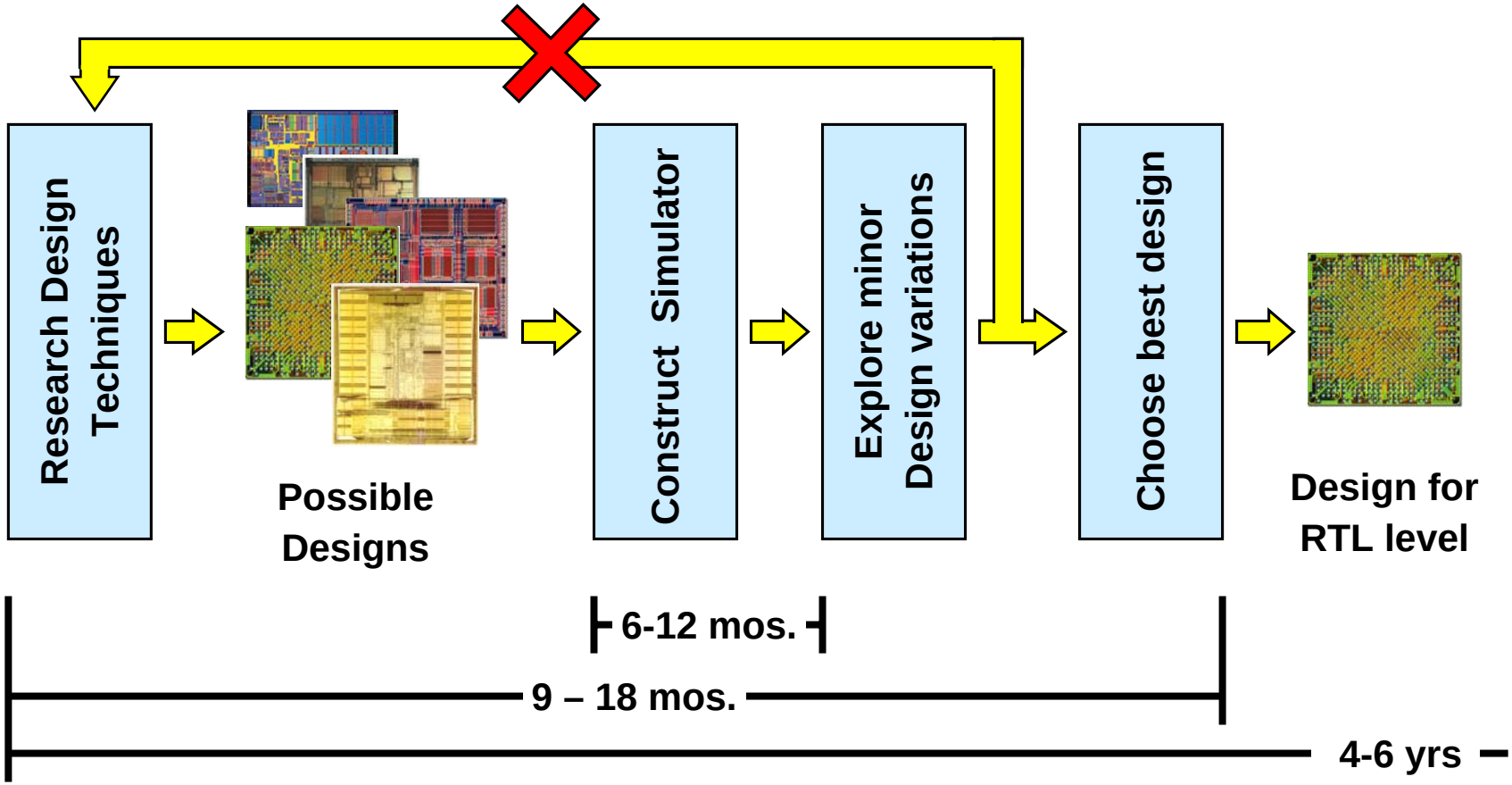
8:00	Welcome	
8:05	LSE Introduction and Philosophy	David
	LSE Basics	Manish
	Your First Configuration	Neil
10:00	Refreshment Break (30 Minutes)	
10:30	Emulators	Manish and Neil
	Building Processor Model	Manish and Neil
	Running OS Code	Jason
	Putting It All Together	David
	The Future of Liberty	David
12:30	Adjourn	

The Hardware Design Process



- Microarchitecture difficult to design
- Design decisions have major implications
- Expensive to correct shortcomings later

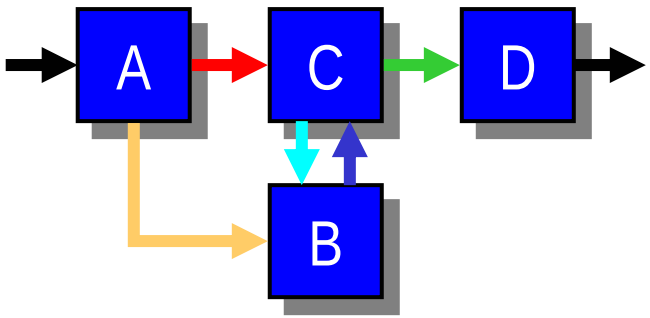
Microarchitecture Design Process



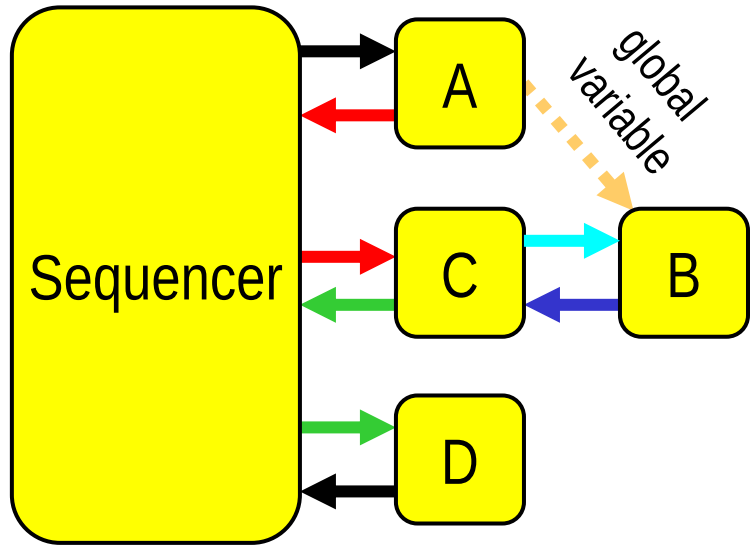
- Only 1 major design concept is tried
  - Only minor variations such as cache size and branch prediction explored
- Simulator is inaccurate [Black '98, Gibson '00, Intel '04]
  - Predictions off by 10%-30%

The Mapping Problem

Hardware Block Diagram



Software Call Graph (C, C++, etc.)

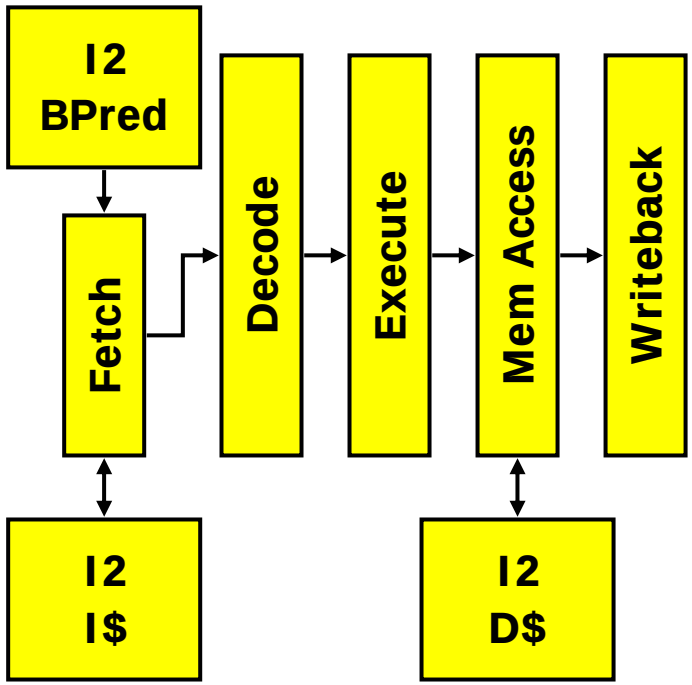


- Equivalent functionality but cognitive mismatch
- No mapping discipline for this manual process
  - error prone
  - time consuming
  - little reuse and interoperability
- C, C++ simulators suffer from this problem (Simics, SimpleScalar)
- Others have remnants of this (ASIM, most SystemC models)

The Mapping Problem in Practice

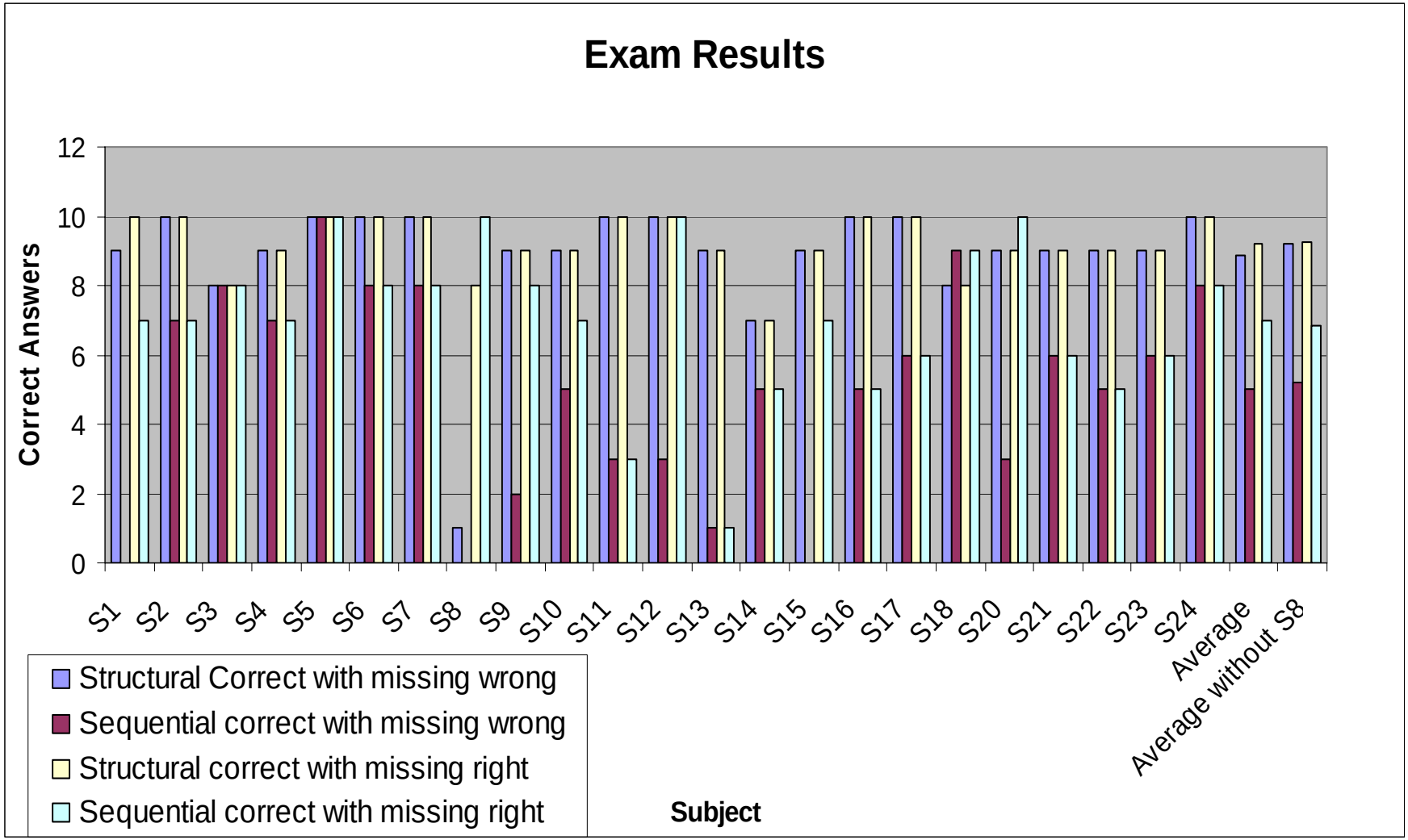
- Must remap to avoid pitfalls [LSE/MICRO35]
  - Locked into major architecture decisions without iteration
  - Hard to keep simulator up-to-date (e.g. VLSI designer feedback)
- Reverse mapping is difficult – Not Transparent
  - Simulators are hard to validate (little trust in simulator results)
  - Simulators do not accurately model the hardware [Hennessy/Flash vs. Flash]
- Temptation to approximate is strong
  - Timing is often approximated, without validation of approximation [Emer/Asim]
- Mapping accuracy important
  - Design details must accurately be modeled to show true performance of architecture [Berger/sim-alpha]

A Natural Specification Language

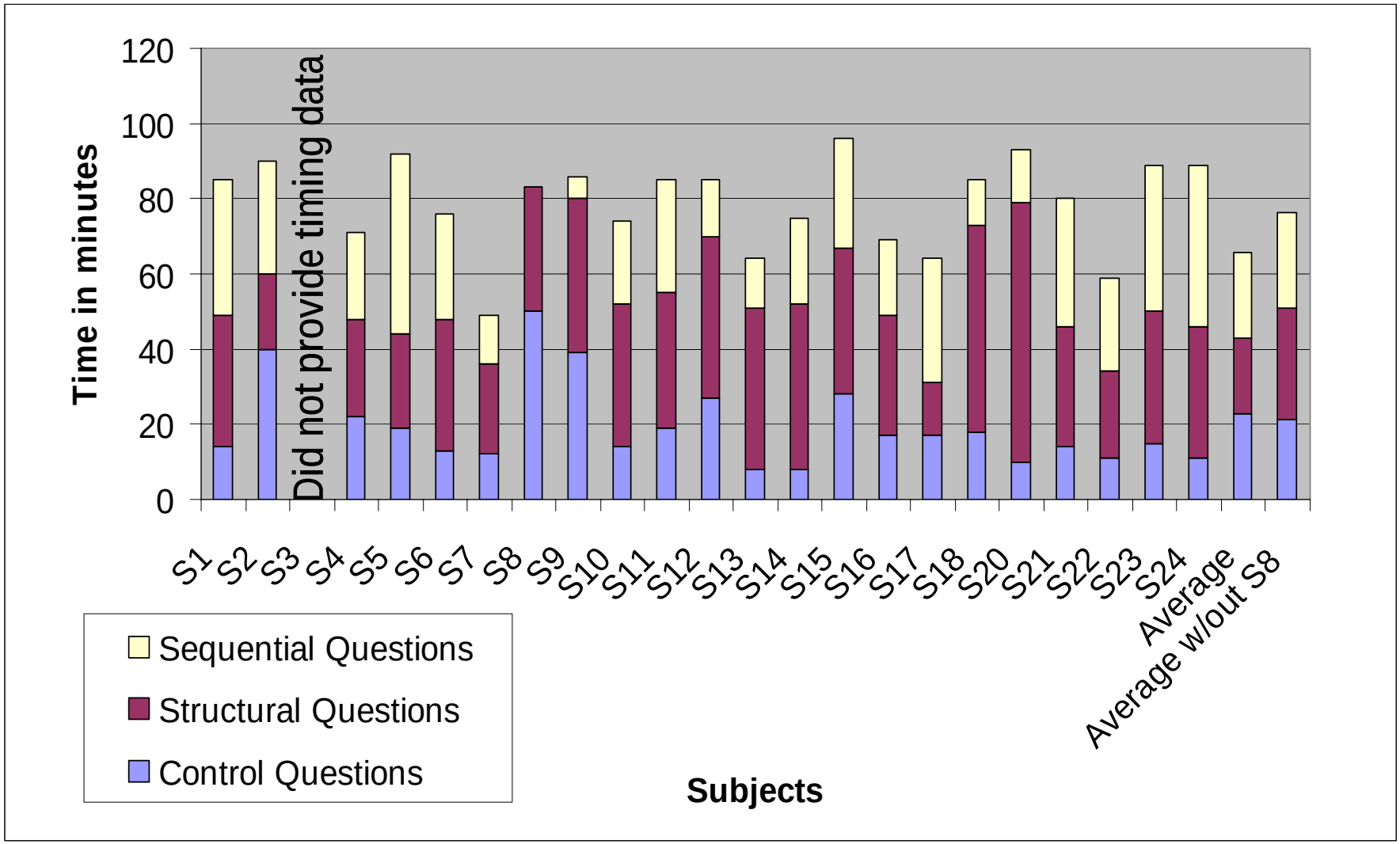


- Modularize the model like hardware, no mapping!
- Basic components
  - Concurrent computation
  - Communication through ports
- Called structural modeling

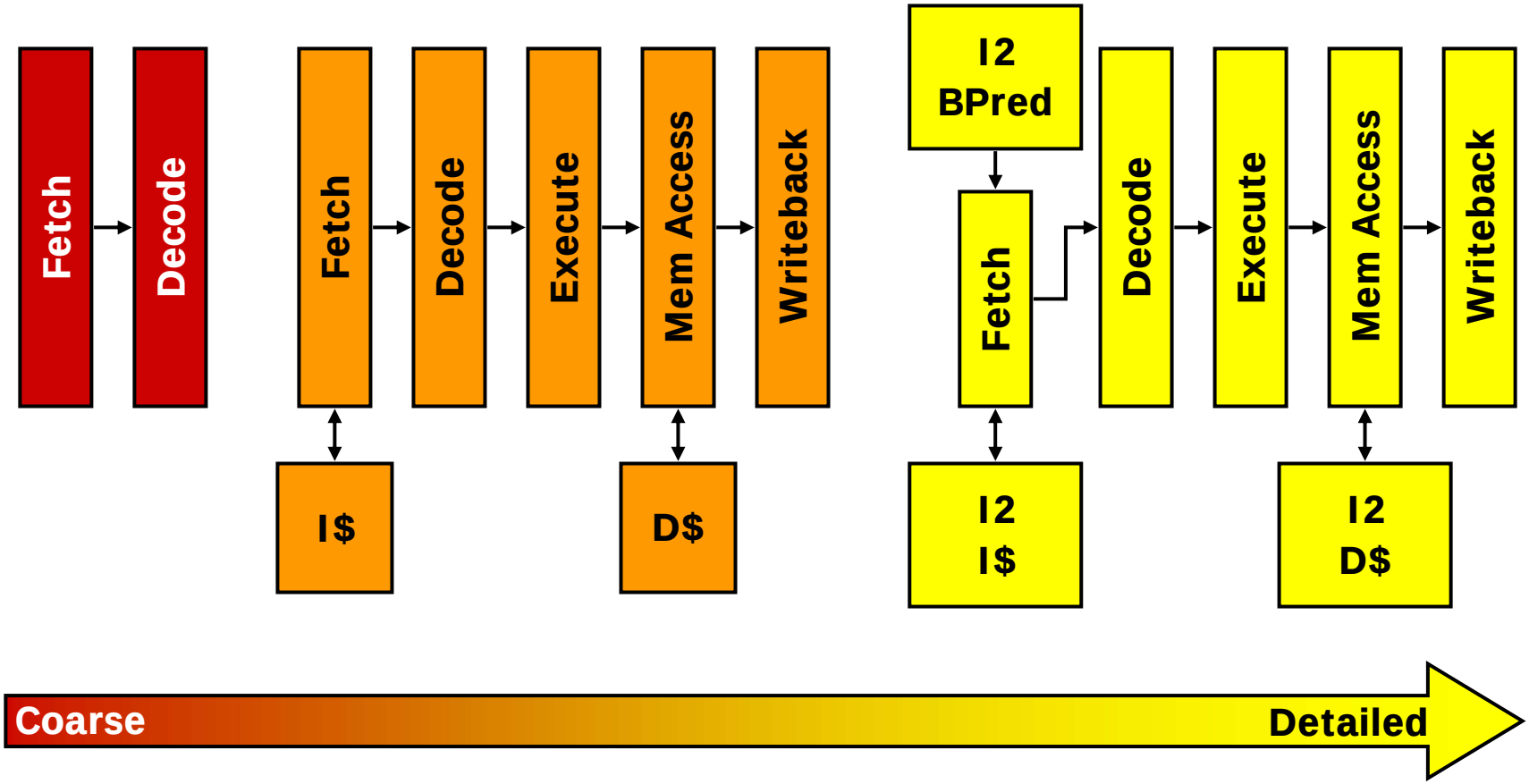
Exam Results



Exam Times

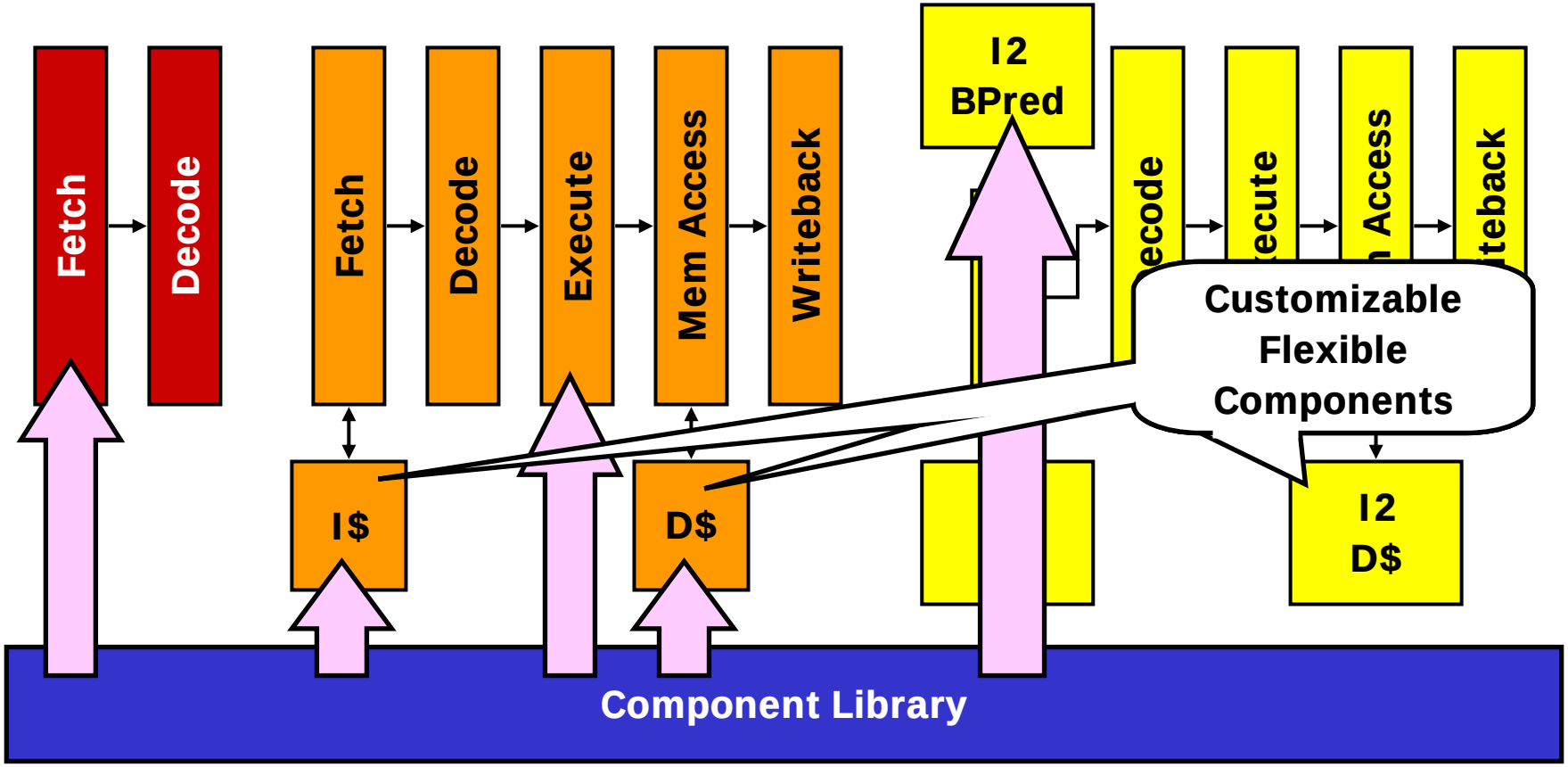

Time in minutes
120
100
80
60
40
20
0
Did not provide timing data
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S20
S21
S22
S23
S24
Average
Average w/out S8
Sequential Questions
Structural Questions
Control Questions
Subjects

Managing Hardware Complexity During Design



- Designers reason about the design through decomposition
- Design is refined by adding and improving components

Accelerate Modeling with Reuse

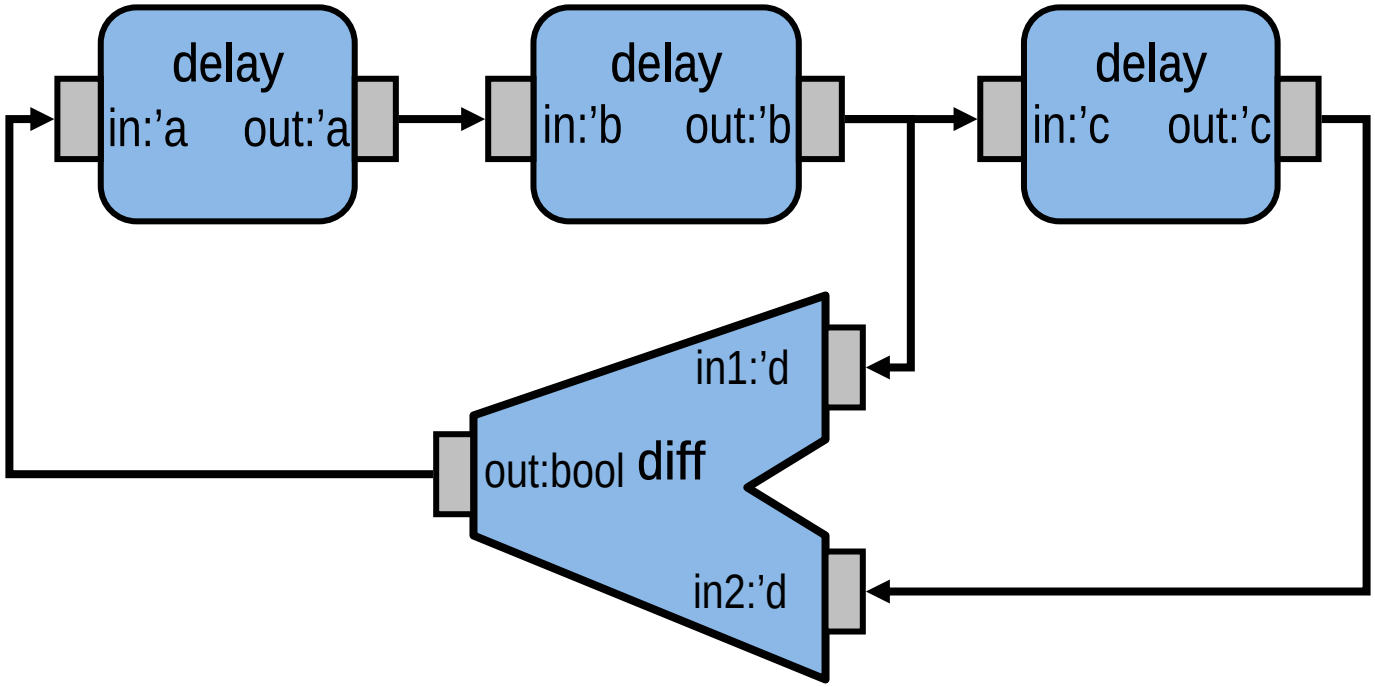


- Reuse components to amortize costs [Charest '02, Emer '02, Koegst '98]
- Real reuse results from structural component use

The Hard Realities of Reuse

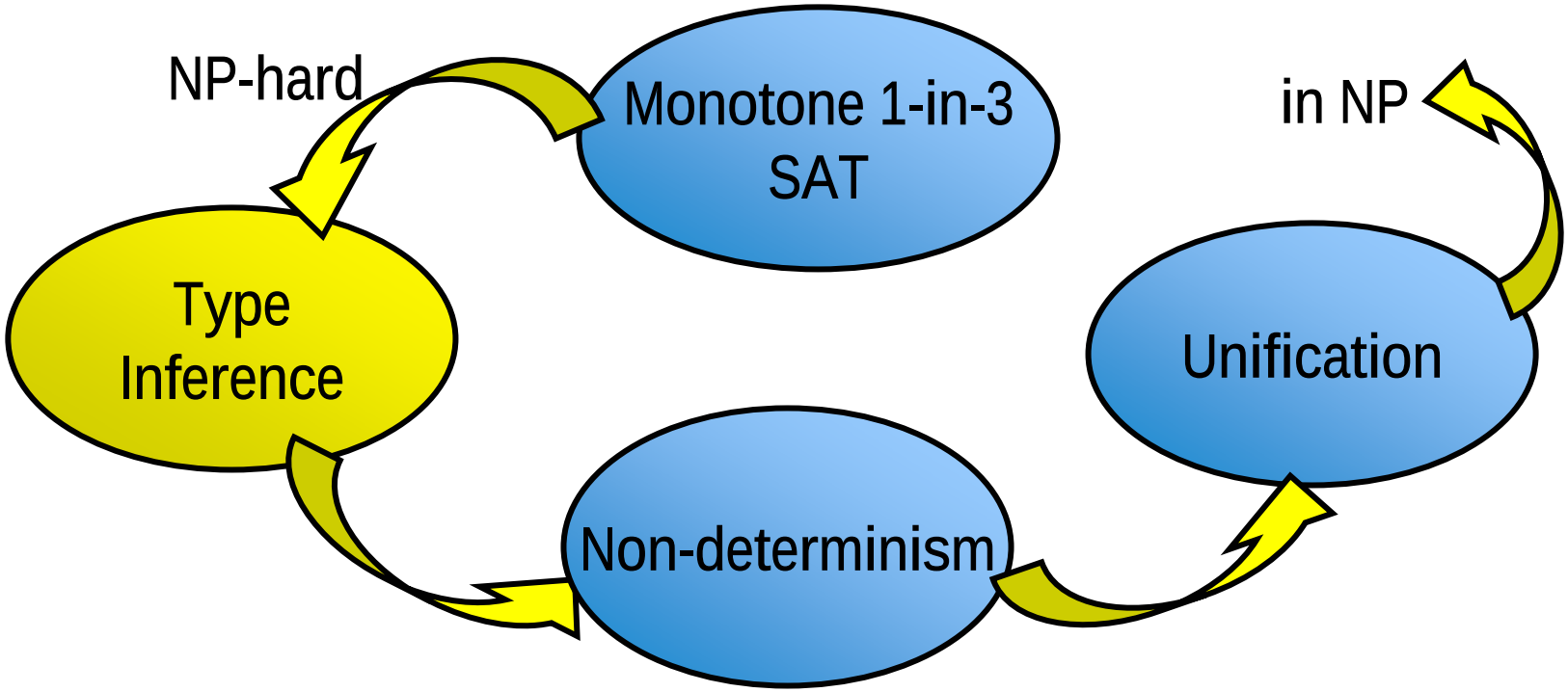
- Cannot reuse blocks that cannot be modularized
  - For example: timing control has global pipeline knowledge
  - LSE: Modularization strategy for timing control
- Reuse overhead too high
  - Reuse requires highly flexible components
  - Flexible components require too much specification [Radetzki '98]
  - LSE: New techniques to infer component parameters
  - LSE: Statically analyzable model structure
  - LSE: Separation of concerns (instrumentation, domains)
- LSE: Don't write a simulator, specify a model

Types Inference via Structure



- Parametric polymorphism can be resolved via static structure
  - `'a = bool, 'b=bool, 'c=bool, 'd=bool`
- Basic algorithm functions by solving constraints
  - Similar to type reconstruction for MinML [Harper '03]

Type Inference is NP-complete [Liberty-04-02]



- Problem is NP-hard
  - Can map any 3-in-1 monotone 3-SAT problem to type inference problem
- Problem is in NP
  - Use non-determinism to decide direction of ‘or’-types
  - Without or-types, problem is unification which is in P [Paterson ’76]

We the People

of the United States, in Order to form a more perfect Union, establish Justice, insure domestic Tranquility, provide for the common Defence, promote the general Welfare, and secure the Blessings of Liberty to ourselves and our Posterity, do ordain and establish this Constitution for the United States of America.

Article. I

Section. 1. All legislative Powers herein granted shall be vested in a Congress of the United States, which shall consist of a Senate and House of Representatives.

Section. 2. The House of Representatives shall be composed of Members chosen every second Year by the People of the several States, and the Electors in each State shall have the Qualifications requisite for Electors of the most numerous Branch of the State Legislature.

No Person shall be a Representative who shall not have attained to the Age of twenty five Years, and been seven Years a Citizen of the United States, and who shall not, when elected, be an Inhabitant of that State in which he shall be chosen.

Representatives and direct Taxes shall be apportioned among the several States which may be included within this Union, according to their respective Numbers, which shall be determined by adding to the whole Number of free Persons, including those bound to Service for a Term of Years, and excluding Indians not taxed, three fifths of all other Persons. The actual Enumeration shall be made within three Years after the first Meeting of the Congress of the United States, and within every subsequent Term of ten Years, in such Manner as they shall by Law direct. The Number of Representatives shall not exceed one for every thirty Thousand, but each State shall have at least one Representative; and until such Enumeration shall be made, the State of New Hampshire shall be entitled to chuse three, Massachusetts eight, Rhode Island and Providence Plantations one, Connecticut five, New York six, New Jersey four, Pennsylvania eight, Delaware one, Maryland six, Virginia ten, North Carolina five, South Carolina five, and Georgia three.

When vacancies happen in the Representation from any State, the Executive Authority thereof shall issue Writs of Election to fill such Vacancies.

The House of Representatives shall chuse their Speaker and other Officers; and shall have the sole Power of Impeachment.

Section. 3. The Senate of the United States shall be composed of two Senators from each State, chosen by the Legislature thereof, for six Years; and each Senator shall have one Vote.

Immediately after they shall be assembled in Consequence of the first Election, they shall be divided as equally as may be into three Classes. The Seats of the Senators of the first Class shall be vacated at the Expiration of the second Year, of the second Class at the Expiration of the fourth Year, and of the third Class at the Expiration of the sixth Year, so that one third may be chosen every second Year; and if Vacancies happen by Resignation, or otherwise, during the Recess of the Legislature of any State, the Executive thereof may make temporary Appointments until the next Meeting of the Legislature, which shall then fill such Vacancies.

No Person shall be a Senator who shall not have attained to the Age of thirty Years, and been nine Years a Citizen of the United States, and who shall not, when elected, be an Inhabitant of that State for which he shall be chosen.

The Vice President of the United States shall be President of the Senate, but shall have no Vote, unless they be equally divided.

The Senate shall chuse their other Officers, and also a President pro tempore, in the Absence of the Vice President, or when he shall exercise the Office of President of the United States.

The Senate shall have the sole Power to try all Impeachments. When sitting for that Purpose, they shall be on Oath or Affirmation. When the President of the United States is tried, the Chief Justice shall preside: And no Person shall be convicted without the Concurrence of two thirds of the Members present.

Judgment in Cases of Impeachment shall not extend further than to removal from Office, and disqualification to hold and enjoy any Office of Honor, Trust or Profit under the United States: but the Party convicted shall nevertheless be liable and subject to Indictment, Trial, Judgment and Punishment, according to Law.

Section. 4. The Times, Places and Manner of holding Elections for Senators and Representatives, shall be prescribed in each State by the Legislature thereof; but the Congress may at any time by Law make or alter such Regulations, except as to the Places of chusing Senators.

The Congress shall assemble at least once in every Year, and such Meeting shall be on the first Monday in December, unless they shall by Law appoint a different Day.

Section. 5. Each House shall be the Judge of the Elections, Returns and Qualifications of its own Members, and a Majority of each shall constitute a Quorum to do Business; but a smaller Number may adjourn from day to day, and may be authorized to compel the Attendance of absent Members, in such Manner, and under such Penalties as each House may provide.

Each House may determine the Rules of its Proceedings, punish its Members for disorderly Behaviour, and, with the Concurrence of two thirds, expel a Member.

Each House shall keep a Journal of its Proceedings, and from time to time publish the same, excepting such Parts as may in their Judgment require Secrecy; and the Yeas and Nays of the Members of either House on any question shall, at the Desire of one fifth of those Present, be entered on the Journal.

Neither House, during the Session of Congress, shall, without the Consent of the other, adjourn for more than three days, nor to any other Place than that in which the two Houses shall be sitting.

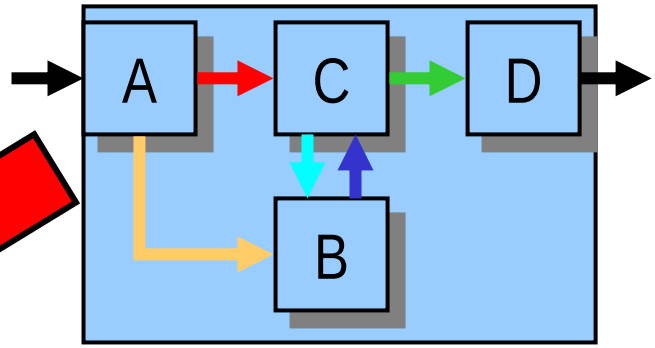
Section. 6. The Senators and Representatives shall receive a Compensation for their Services, to be ascertained by Law, and paid out of the Treasury of the United States. They shall in all Cases, except Treason, Felony and Breach of the Peace, be privileged from Arrest during their Attendance at the Session of their respective Houses, and in going to and returning from the same; and for any Speech or Debate in either House, they shall not be questioned in any other Place.

No Senator or Representative shall, during the Time for which he was elected, be appointed to any civil Office under the Authority of the United States, which shall have been created, or the Emoluments whereof shall have been encreased during such time; and no Person holding any Office under the United States, shall be a Member of either House during his Continuance in Office.

Section. 7. All Bills for raising Revenue shall originate in the House of Representatives; but the Senate may propose or concur with Amendments as on other Bills.

Every Bill which shall have passed the House of Representatives and the Senate, shall, before it become a Law, be presented to the President of the

LSE: Natural Specification



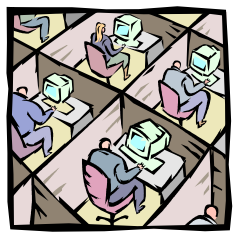
Simulator Specification

μ-arch Specification

Component Library

Description Compiler

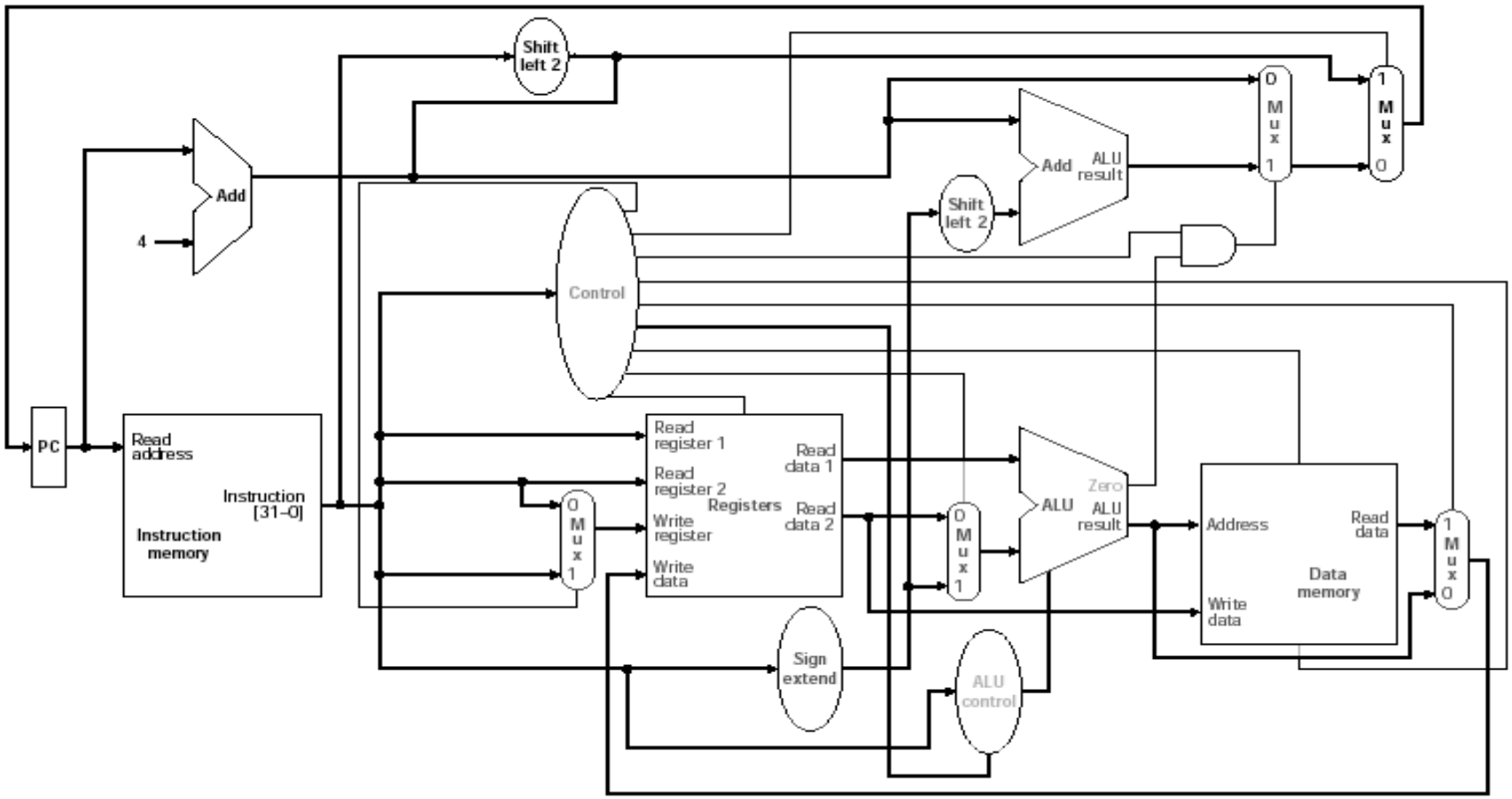
Executable Simulator



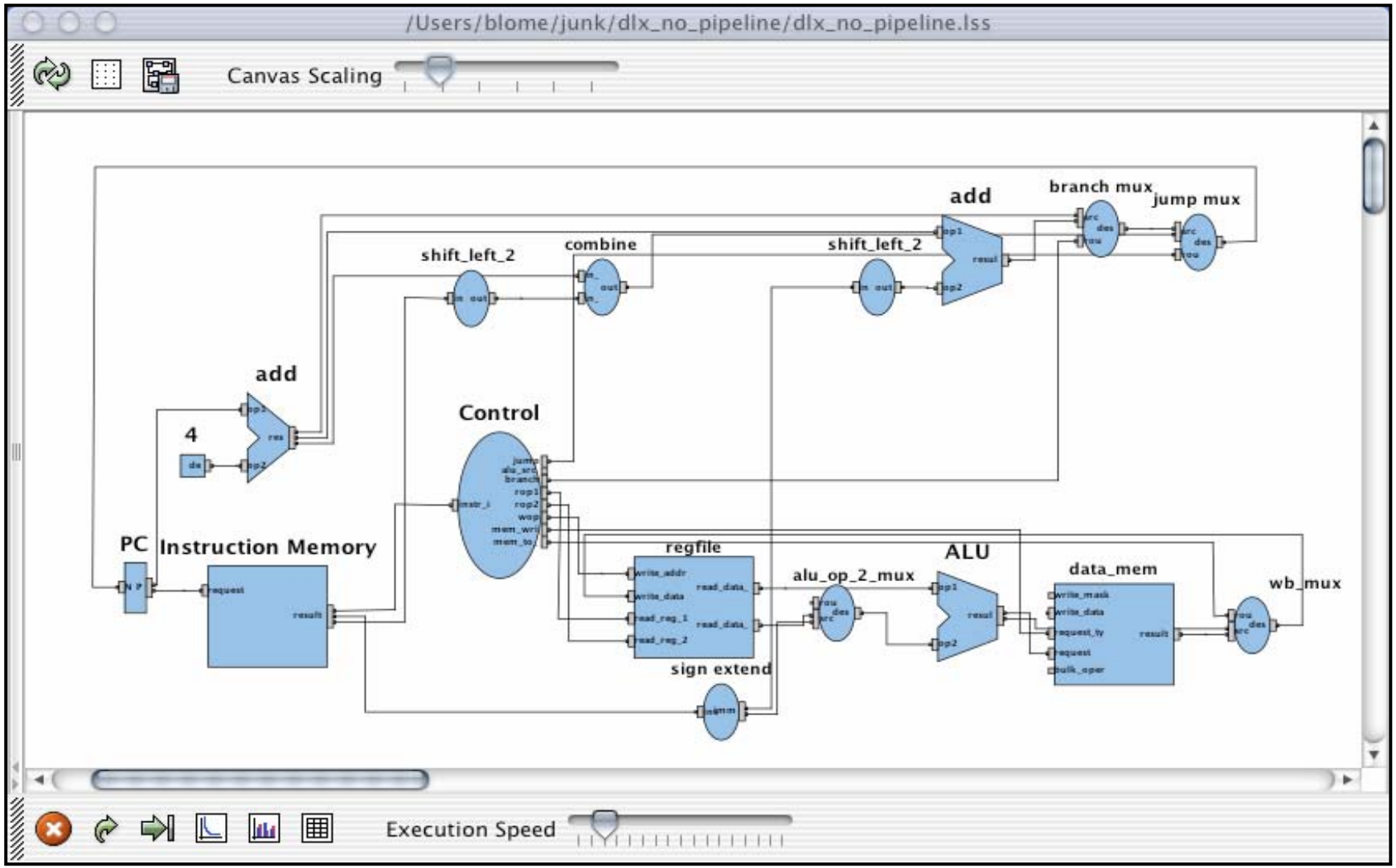
- Eliminates mapping problem
- No preconceived ideas
- Amortize costs
  - Reuse Components [Charest '02, Emer '02, Koegst '98, Radetzki '98]
  - Enabled by structural specification [MICRO-35, PLDI '04]

Analyzability and Communication of Ideas

Figure from H&P

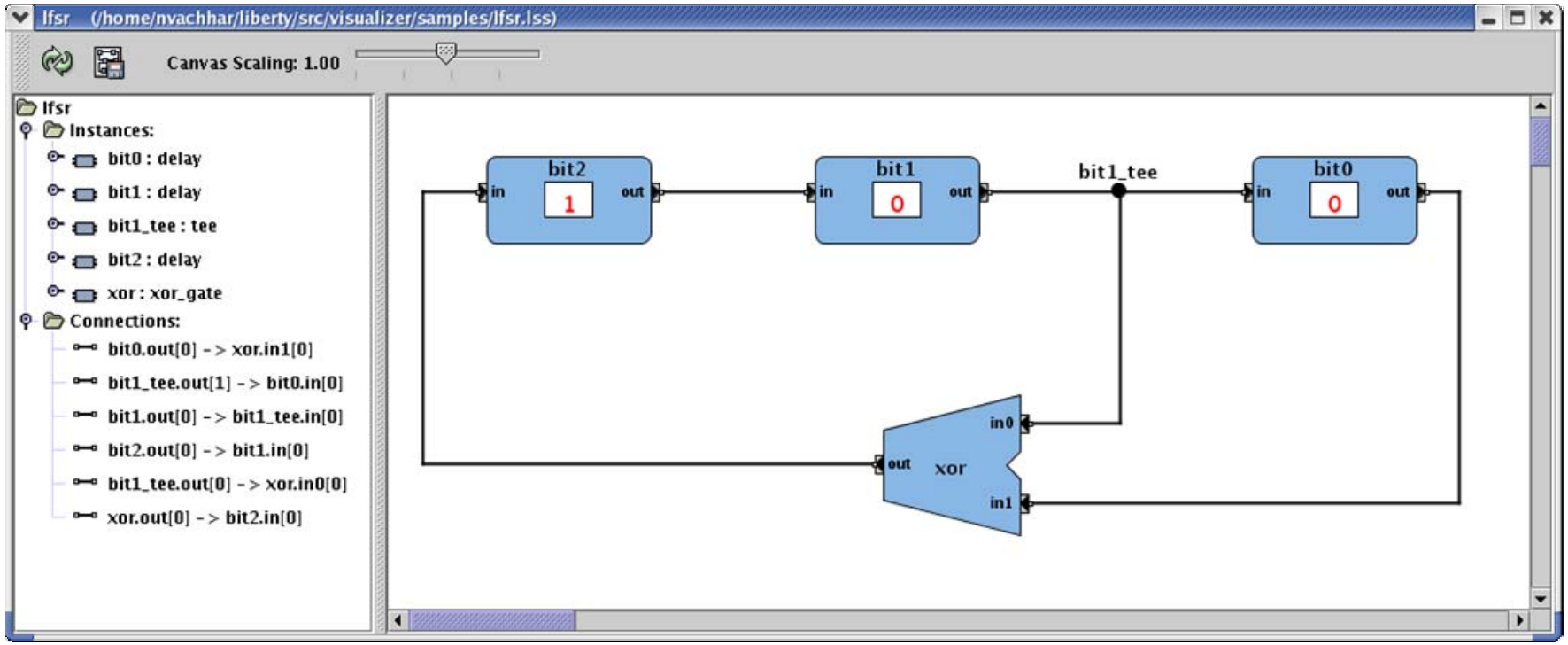


Analyzability and Communication of Ideas Automatically Generated



Analyzability and Communication of Ideas

Automatically Generated



Reuse

LSE allows for user-defined modules, but...

LSE comes with some libraries:

- Core components, examples:
  - arbiter - Arbitrate anything with any policy
  - mqueue - Multiple in/out queue of any type
  - router - Route anything with any policy
  - sink - Think /dev/null of any type
  - source - Universal source of any pattern and type
- Architectural components, examples:
  - Cache Replacement Controller - Any replacement policy
  - Cache Request Module - Any request structure

Reuse Across Models in LSE

Model	Instances	Hierarchical Modules	Leaf Modules	Instances/ Module	% Instances from Library	Library Modules
A	277	46 (10)	18	4.33 (8.61)	73%	13
B	281	46 (11)	18	4.39 (8.48)	73%	12
C	62	1	18	3.37	73%	10
D	192	4	25	6.62	86%	22
E	329	4	26	10.97	89%	22
F	183	18(3)	19	4.35 (8.32)	82%	18
Total	1324	69 (16)	39	12.26 (22.83)	80%	22

- A – Tomasulo style machine that executes DLX instructions
- B – Same as A but with a unified issue window
- C – Model equivalent to Simplescalar's sim-outorder.c machine
- D – Out-of-order IA64 core
- E – Two of the OoO IA64 cores communicating with a shared memory
- F – Validated Itanium 2 model

Flexibility

LSE can model anything with a clock
(GALS with the addition of multiple clock domains)

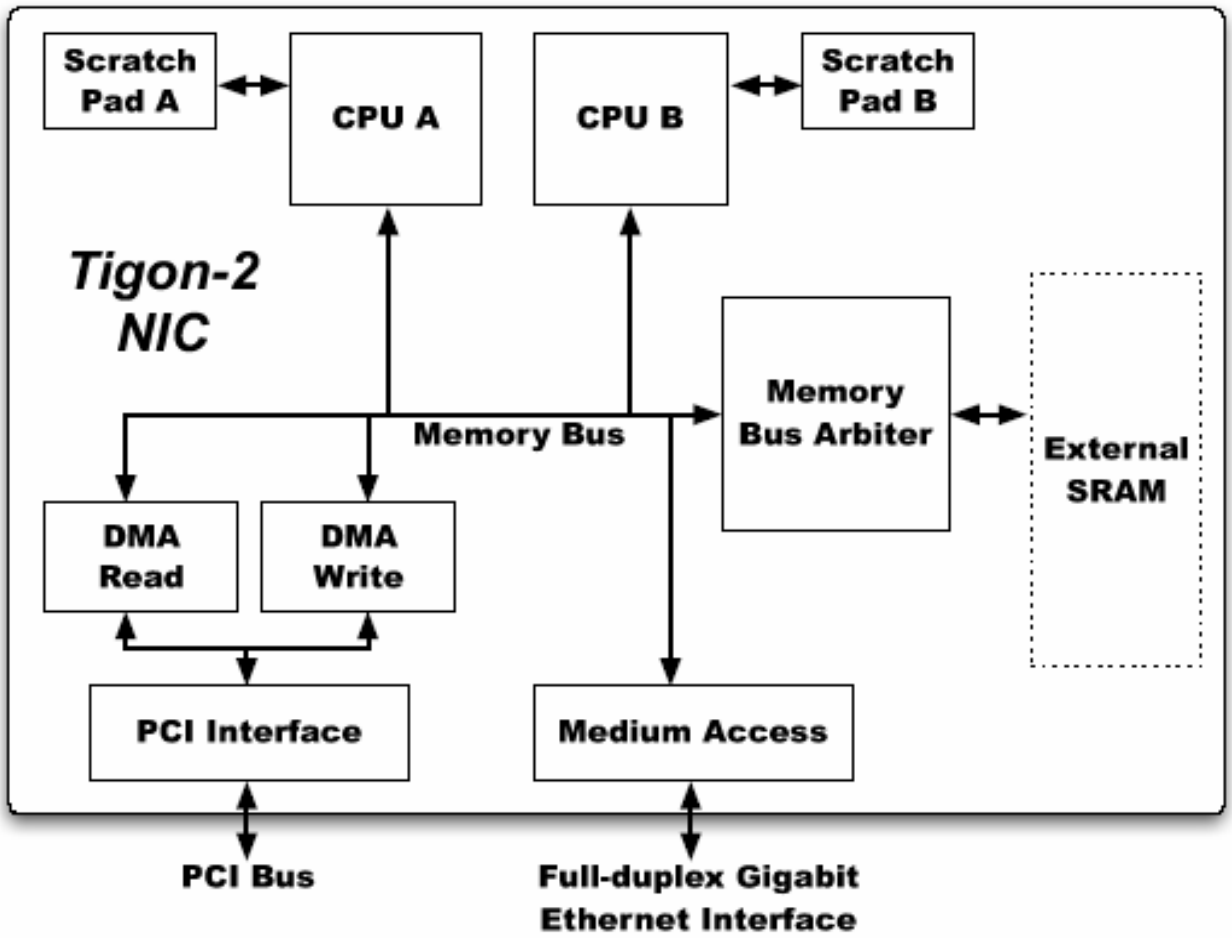
Existing Models From Users Domestic and International:

- Single and multiple core processors OOO/Inorder
- Heterogeneous multiprocessor systems
- Power models of interconnection networks (ORION)
- Toy configurations like LFSR (good for tutorials)
- Variety of DLX processors (LSE concept illustration)
- Multicore network interface controller (SPINACH)
- Tiled and Novel Architectures
- Novel VLIW with Power Models (Justice)
- Flexible Component Sets (MicroLib)

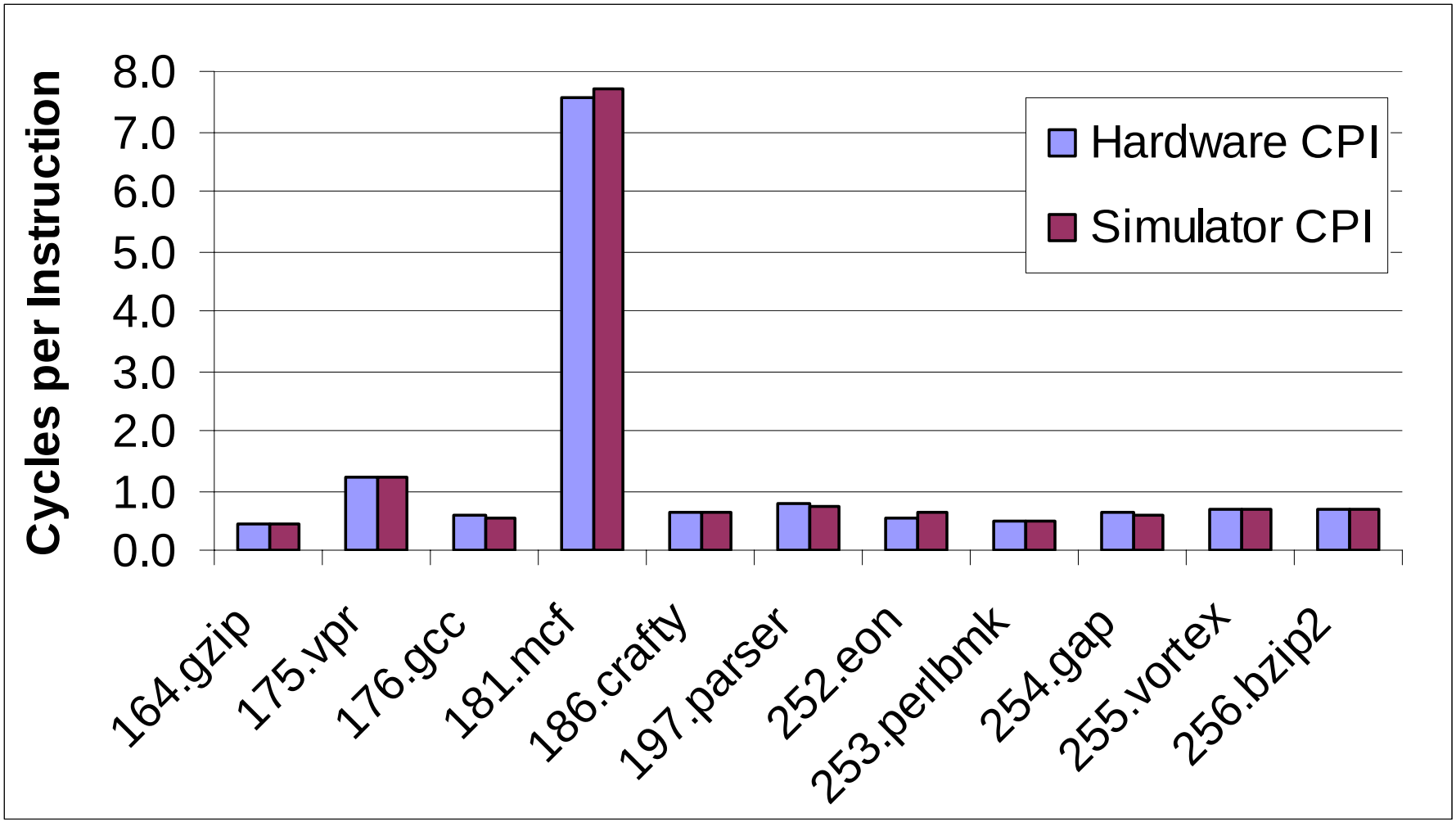
LSE in Practice: Rice University, SPINACH Project

TIGON-2 NIC LSE Model

- Validated TIGON-2 NIC model by Rice University [Willmann, LCTES '04]
- Model constructed by 2 students in 1.5 months (~12 person-weeks)!



LSE in Practice: An Itanium 2 Simulator with LSS



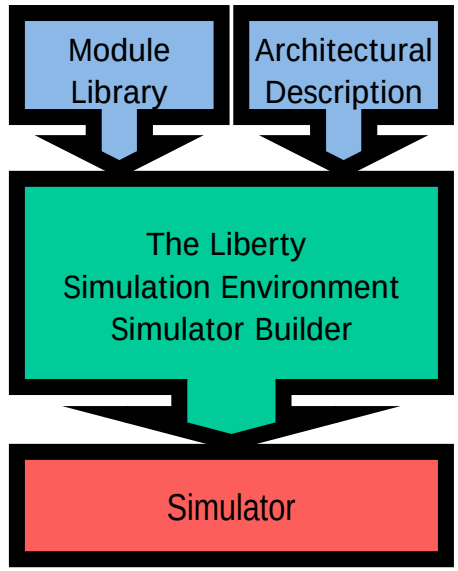
- Itanium 2 simulator built using LSS by one person in 11 weeks!
- Average accuracy within 3% of actual hardware

Simulation Speed of LSE

LSS has an Optimizing Compiler:

- Emits HSR (Heterogeneous Synchronous Reactive) simulator [Edwards '97]
- Optimizes system to create static schedules where possible [DAC '03]
- Eliminates the reuse penalty:

Model	Cycles/sec	Speedup	Build (sec)
Custom SystemC	53722	0.35	49.1
Custom LSE	154104	-	15.4
Reusable LSE	40649	0.26	33.9
Reusable LSE with optimization	57046	0.37	34.4



10x SimpleScalar, but this is just a start to what can be done.

Does this even matter?

Simulation Speed of LSE
Checkpointing and Sampling Domain

- LSE domain supports a variety of checkpointing and sampling methodologies
- TurboSMARTS [Wunderlich et al. ISCA '03] in validated Itanium 2
  - Accurate simulation results – < 3% IPC error, 97% confidence
  - Less time than running code on real hardware!
- Other sampling and checkpointing methodologies supported.

Planned:

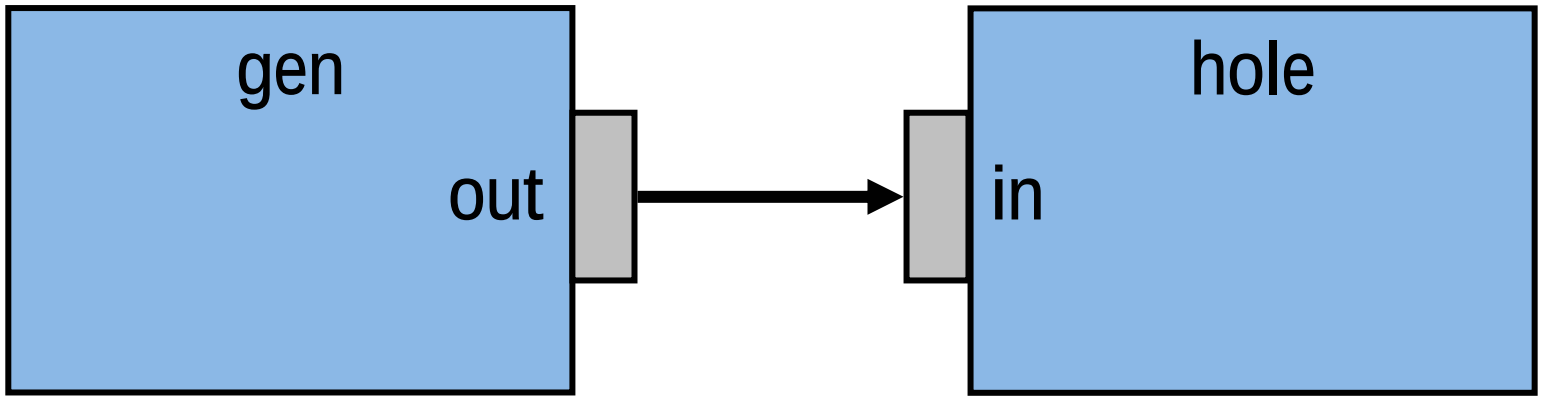
- Additional simulator builder optimizations
- HW assist methods

LSE Key Points Review

- Models built using LSE are accurate
  - 10-30% error → 3% error
  - Independent efforts, same result (TIGON-2 and Itanium 2)
- Building LSE models can be inexpensive
  - Many person-years → few person-months (TIGON-2, Itanium 2)
  - Reuse features that actually get used
- Models are analyzable and meaningful
  - Communicate hardware ideas easily
  - Automatic Visualization
  - Faster simulation with optimization and sampling support

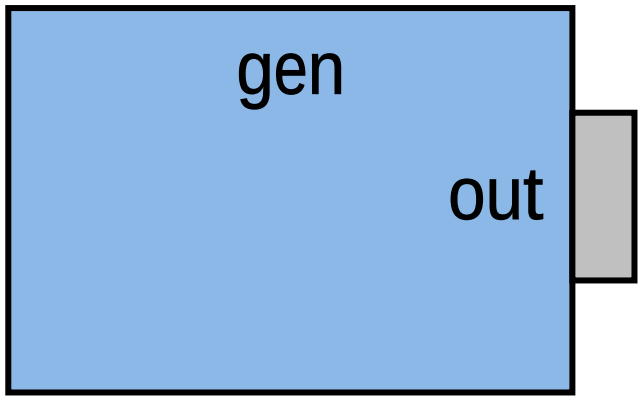
LSE Basics

A Simple Machine



- Model a hardware system at the high-level in which
  - gen outputs a different integer every cycle
  - hole consumes the integer data sent
- Three-options
  - Build a C simulator that models this hardware
  - Write gen and hole components for a modeling system
  - Customize reusable components to build gen and hole

Source Module



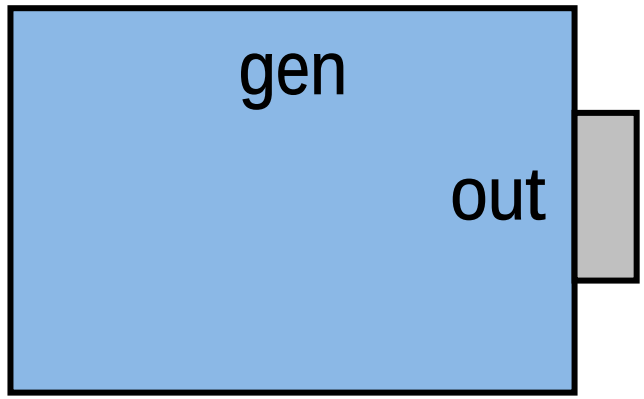

```
using corelib;

instance gen:source;
…
```

LSS specification

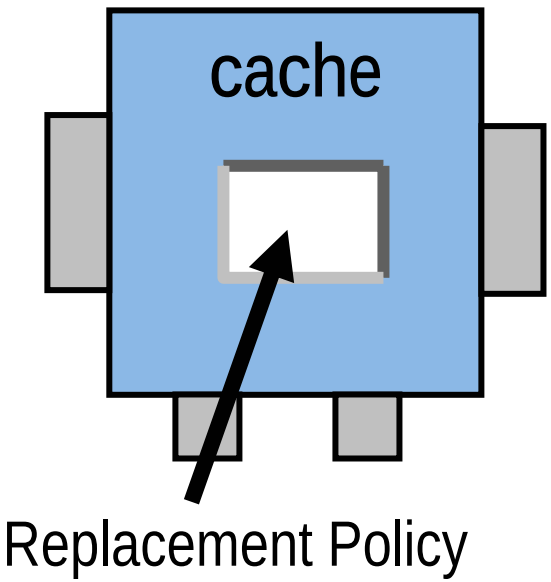
- LSE module library – package corelib
- The **`source`** module
  - Generates one data item per cycle
  - Data type and actual data produced are customizable
- Instantiate the **`source`** module with the name gen

Customizing Modules

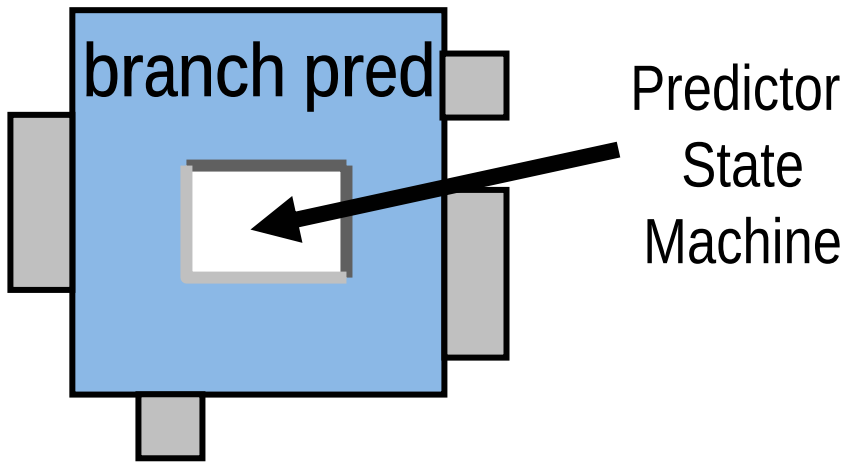
- Conventional Parameters
  - Size of caches
  - History bits in a branch predictor
  - Number of functional units in a processor core
- Source module can use array of data parameter
  - What about constant values?
  - What about infinite sequences?



Algorithmic Parameters

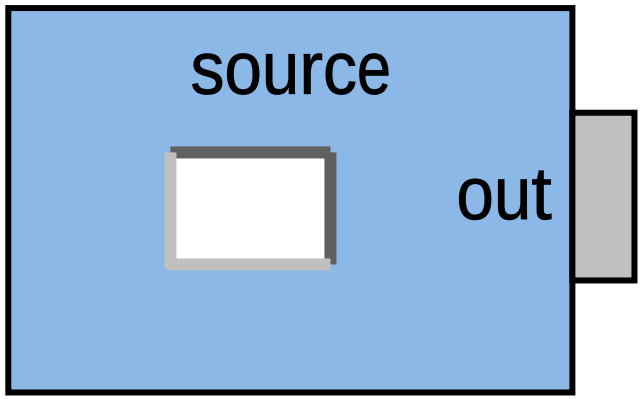


- LSE supports algorithmic parameters
- Called userpoints
- “hole” in module behavior
- Users fill hole to customize
  - Sequential code
  - Good for algorithms



Customizing Modules

Algorithmic Parameters



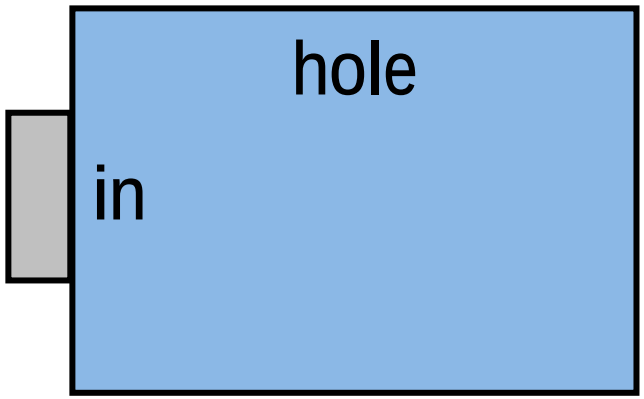

```
module source {
  …
  parameter create_data:
    userpoint(…);
};
```

- Source module
  - `create_data` userpoint - controls data output

Customize Source Behavior

```
using corelib;

instance gen:source;

gen.create_data = <<<
 *data = LSE_time_get_cycle(LSE_time_now);
 return LSE_signal_something | …
   …
>>>;
…
```

Sink Module

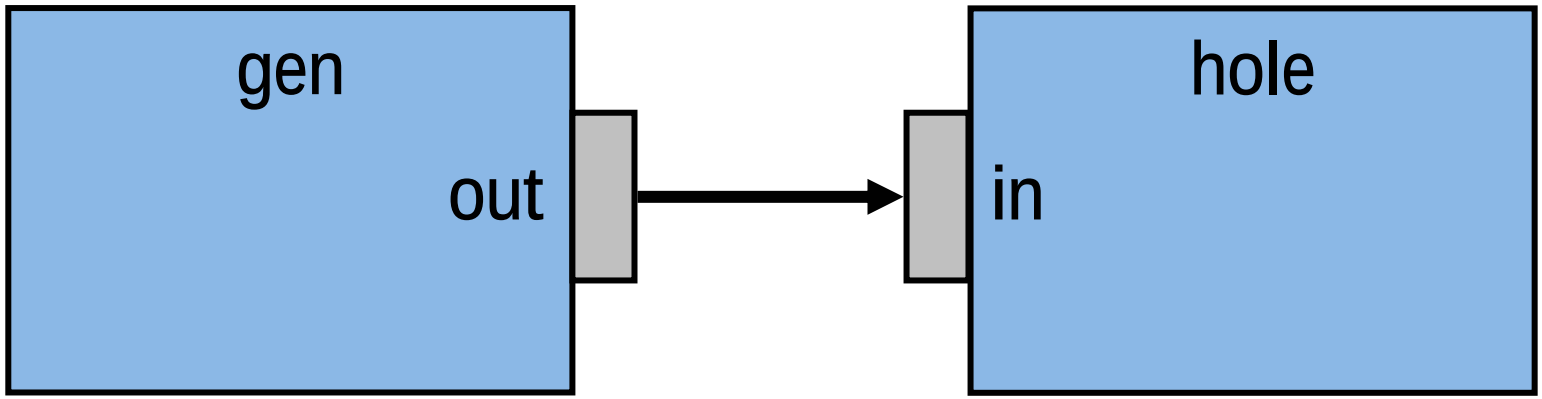



```
using corelib;

instance gen:source;
instance hole:sink;
…
```

LSS specification

- LSE module library – package corelib
- The **`sink`** module
  - Consumes one data item per cycle
- Instantiate the **`sink`** module with the name hole

Building Structure




```
using corelib;

instance gen:source;
… /* create_data code */
instance hole:sink;

gen.out -> hole.in;
```

LSS specification

- Connect gen.out to hole.in

Clock Domains

- Current release supports single synchronous clock
- Next release of LSE will support multiple clocks

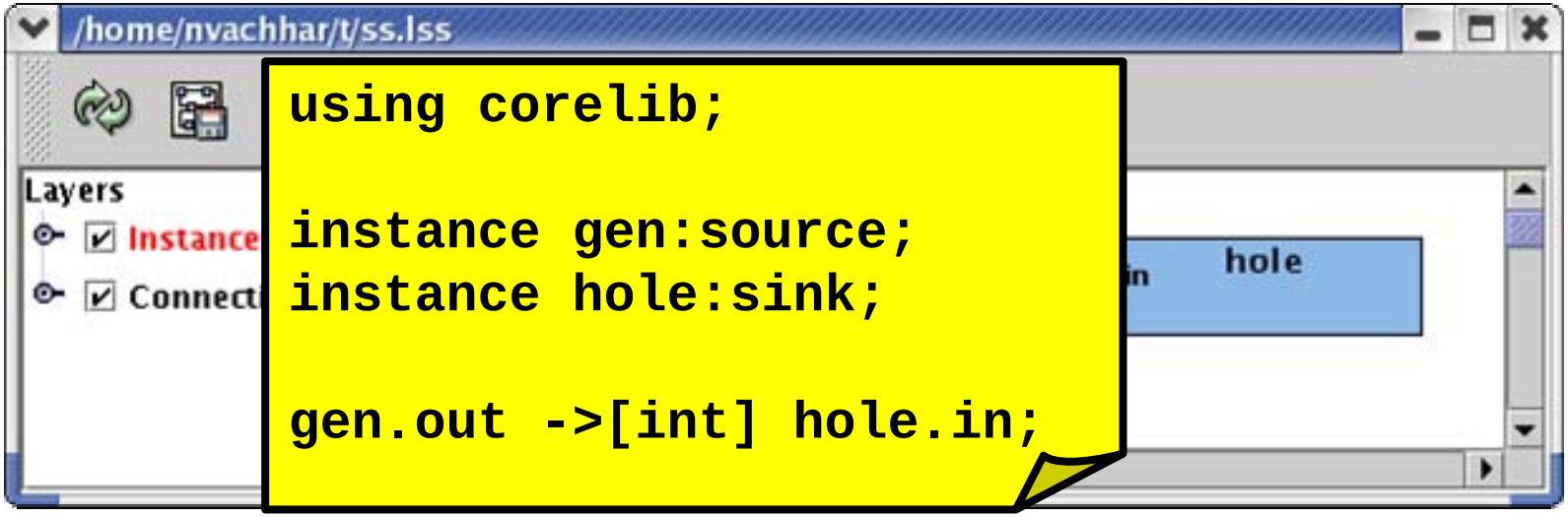
- Instantiate clocks

```
LSE_clock::create("clock1", 100, 0)
LSE_clock::create("clock2", 35, 50)
```

- Assign module instances a clock (or multiple clocks for boundary modules)

- System automatically manages scheduling and time management

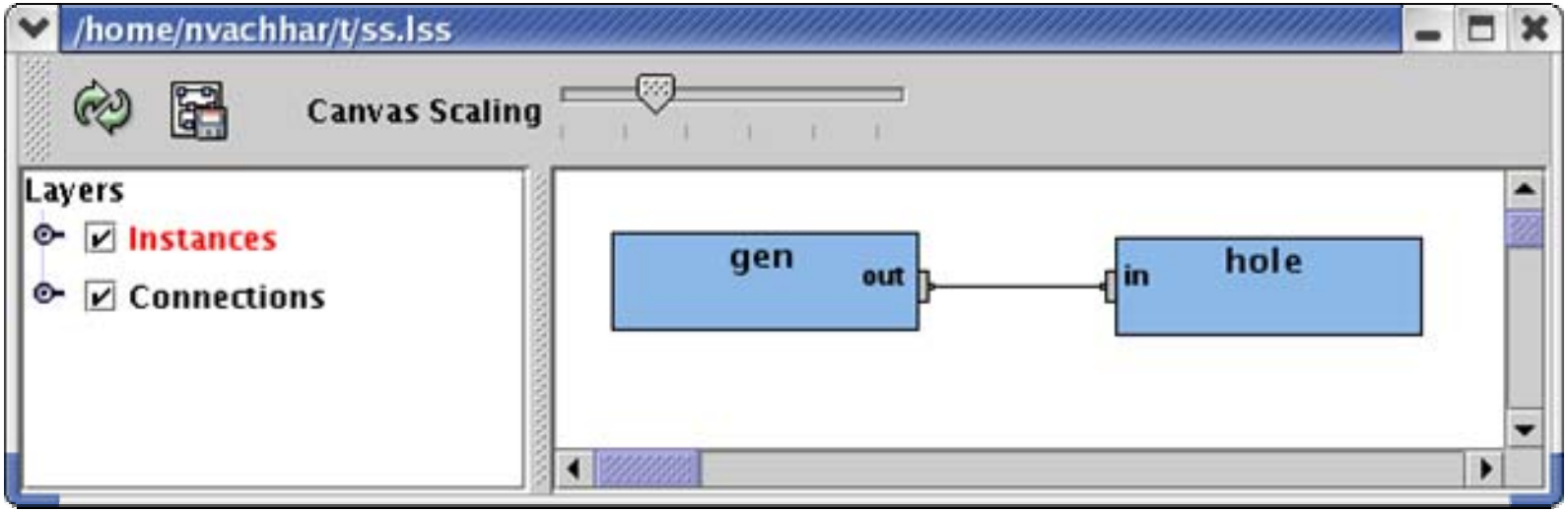
Source-Sink Configuration



- LSE visualizer
  - can automatically visualize specifications
- Model writers mental picture automatically generated!

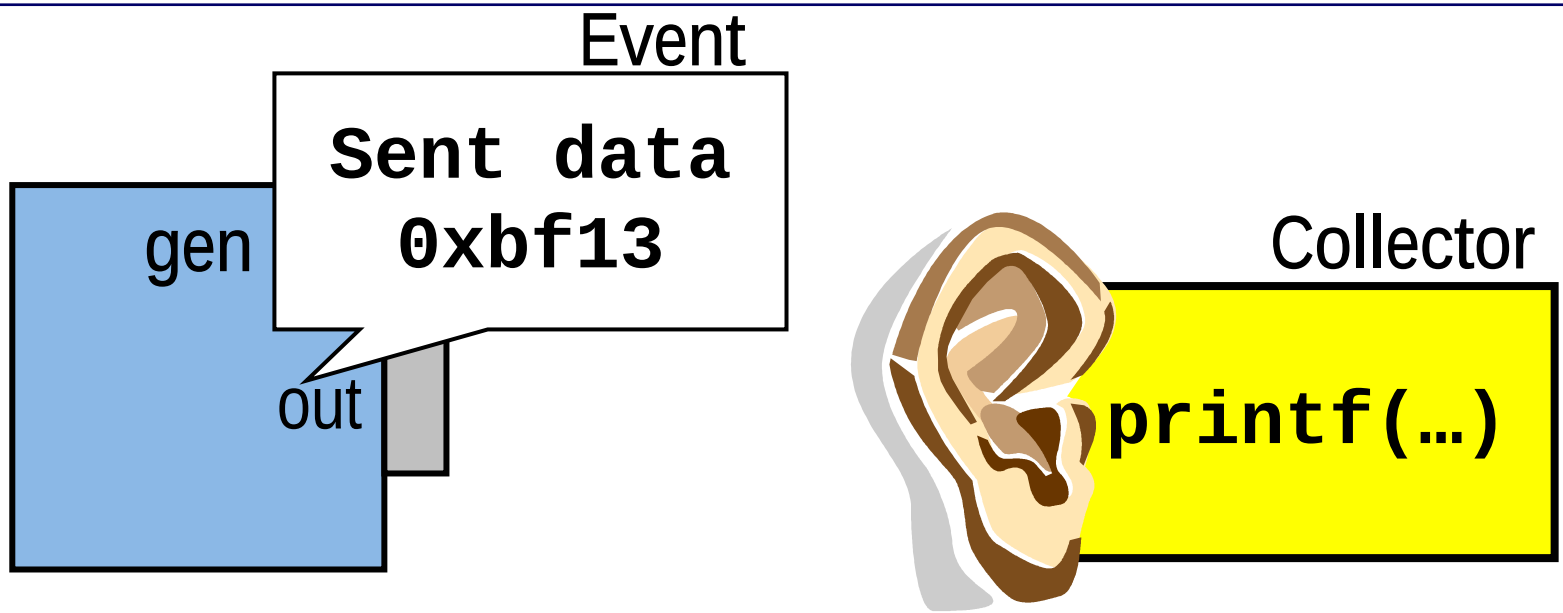
Simulator Instrumentation

Simulator Instrumentation



- What is the output?
- In existing systems
  - Hack the source or sink module to add monitoring code
  - Breaks modularity and reuse
  - Intertwines functionality and instrumentation

Simulator Instrumentation (2)



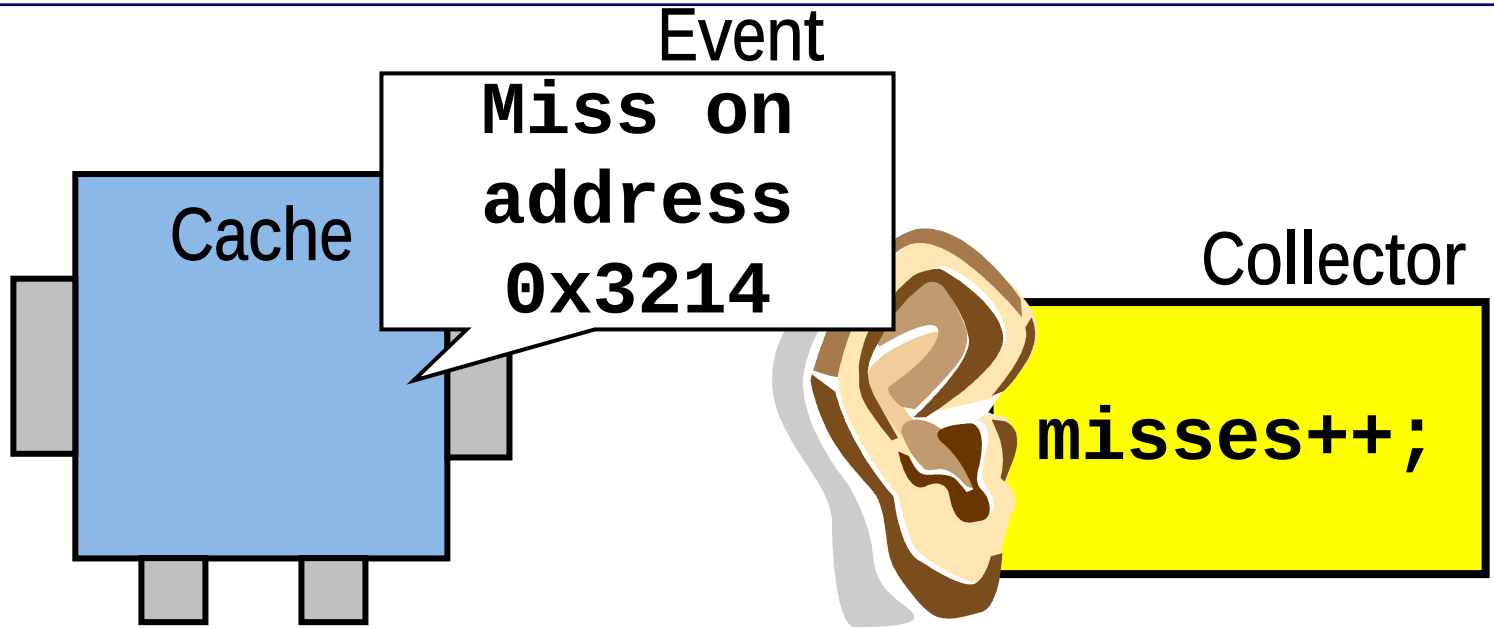

```
collector out.resolved on "gen" {
  record = <<<
    …
    printf(LSE_time_print_args(LSE_time_now));
    printf(": %d\n", *datap);
    …
  >>>;
};
```

Simulator Instrumentation (3)

```
collector out.resolved on “gen” {
  record = <<<
    …
    printf(LSE_time_print_args(LSE_time_now));
    printf(“: %d\n”, *datap);
    …
  >>>;
};
```

```
0/0: 0
1/0: 1
2/0: 2
…..
<CTRL-C>
%
```

Instrumentation Benefits

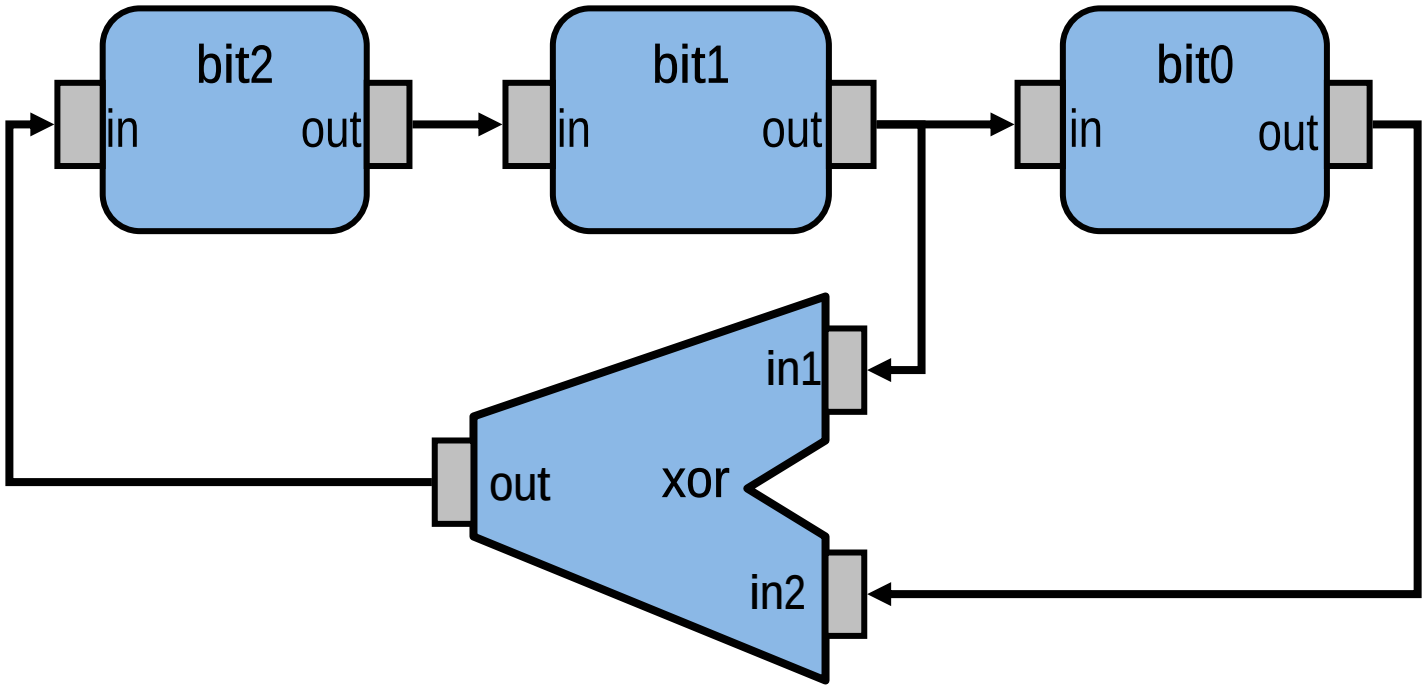


- Instrumentation separate from behavior
- Different users can reuse model
- Components can be reused
  - Data collection code has global knowledge
  - Orthogonality preserves encapsulation

More Complex Configuration

More Complex Configuration

Linear Feedback Shift Register (LFSR)

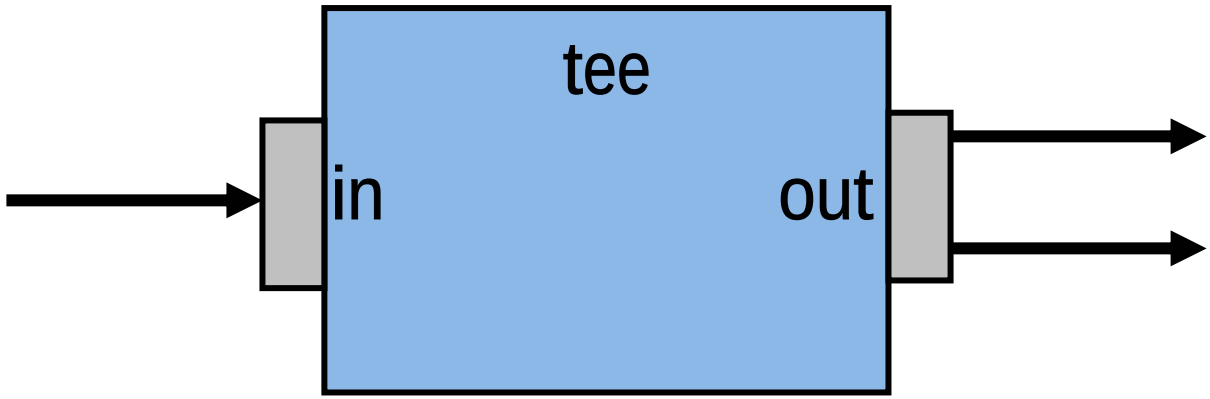


- Built using reusable modules in **`corelib`**
- **`bit0, bit1, bit2`**
  - unit delay modules, called **`delay`**

LFSR Specification

```
using corelib;
include "xor.lss";

instance bit0 : delay;
instance bit1 : delay;
instance bit2 : delay;
instance xor : xor_gate;
instance bit1_tee : tee;

bit2.out -> bit1.in;
bit1.out -> bit1_tee.in;
bit1_tee.out[0] -> xor.in0;
bit1_tee.out[1] -> bit0.in;
bit0.out -> xor.in1;
xor.out -> bit2.in;
```

The tee Module



- Fans out input to multiple outputs
- # of connections to out determines fan-out degree
- Each port in LSE is an array of ports
  - `out` – port
  - `out[i]` – port instance

Ports and Port Instances

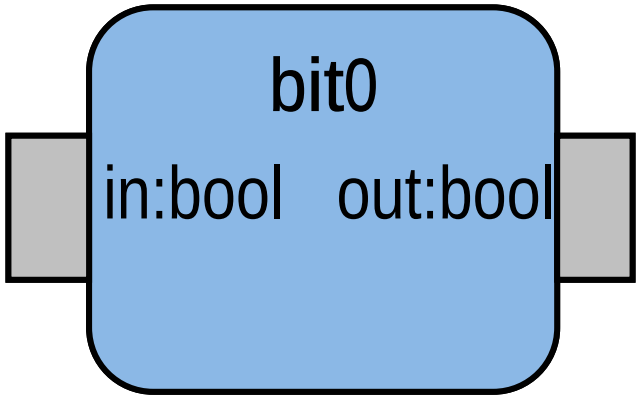
```
using corelib; include
   "xor.lss";

instance bit0 : delay;
instance bit1 : delay;
instance bit2 : delay;
instance xor : xor_gate;
instance bit1_tee : tee;

bit2.out -> bit1.in;
bit1.out -> bit1_tee.in;
bit1_tee.out[0] -> xor.in0;
bit1_tee.out[1] -> bit0.in;
bit0.out -> xor.in1;
xor.out -> bit2.in;
```

Ports and Port Instances

```
using corelib; include
   "xor.lss";

instance bit0 : delay;
instance bit1 : delay;
instance bit2 : delay;
instance xor : xor_gate;
instance bit1_tee : tee;

bit2.out -> bit1.in;
bit1.out -> bit1_tee.in;
bit1_tee.out -> xor.in0;
bit1_tee.out -> bit0.in;
bit0.out -> xor.in1;
xor.out -> bit2.in;
```

Linear Feedback Shift Register
Live Demo

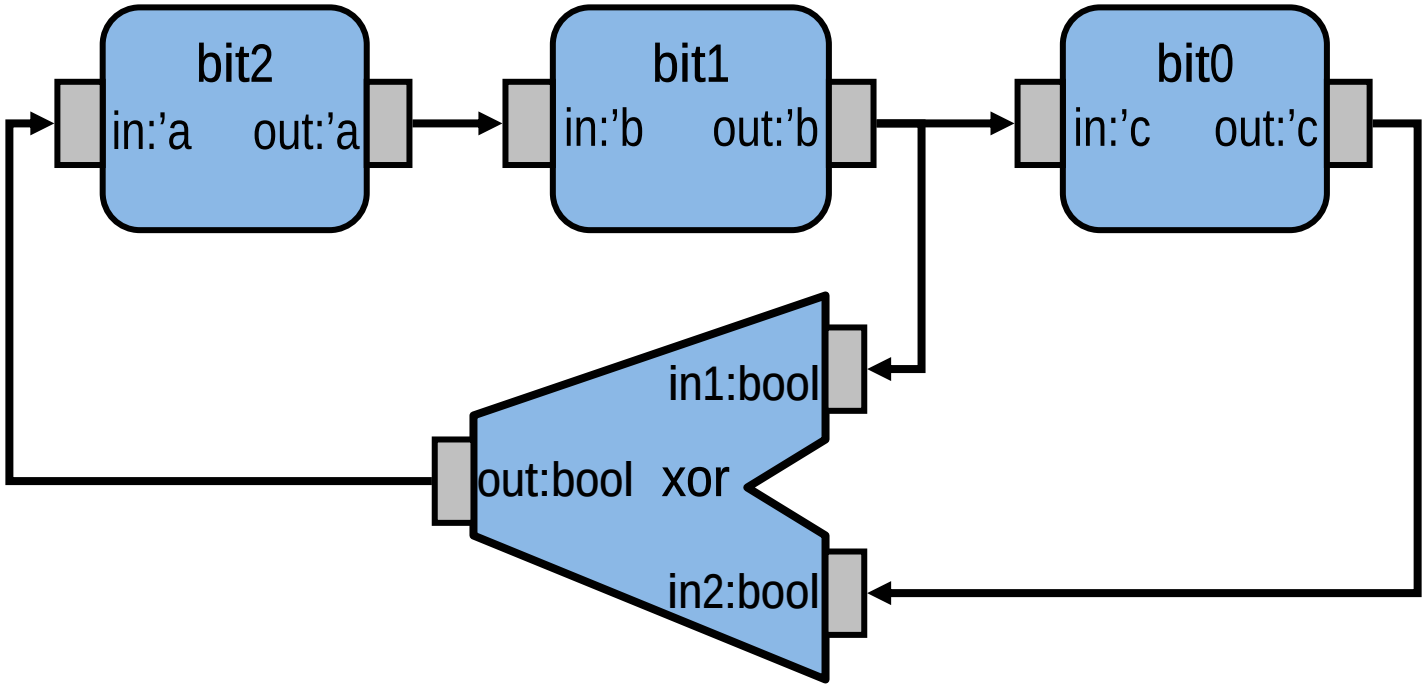
What About Data Types?



- LSE Components can be polymorphic
  - Support more than one datatype
- Polymorphism allows type neutral modules
  - Flexible, reusable, queues, memories, crossbars, etc.
- Delay module
  - Can store data of any type
  - But, only one type per instance at run-time

Polymorphism

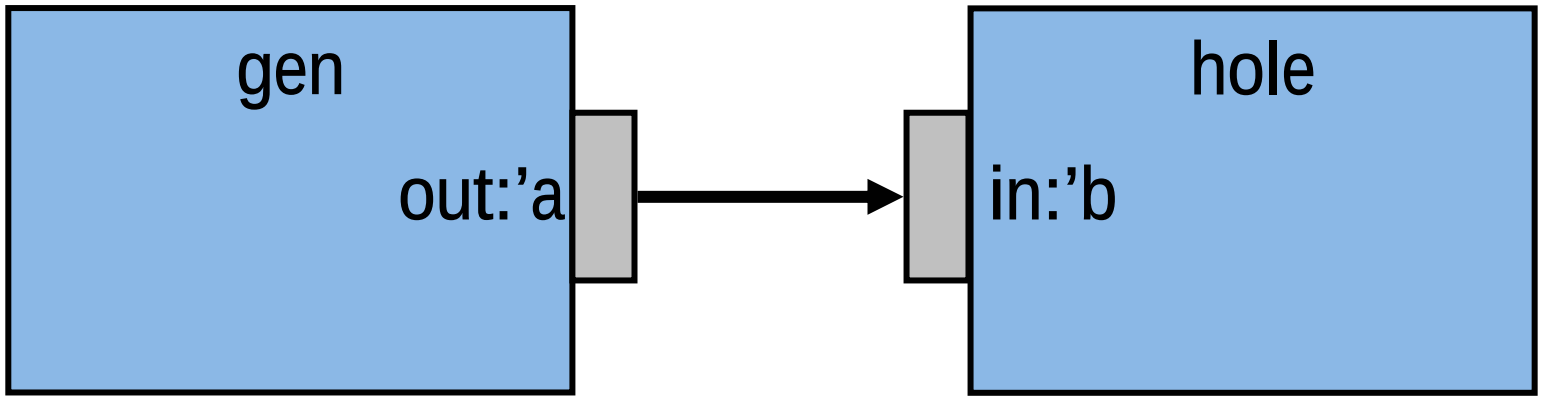
Type Inference



- Explicit instantiation burdensome
- Polymorphism resolved through type inference
  - Reduces cumbersome type instantiation process
- `'a = bool, 'b=bool, 'c=bool`

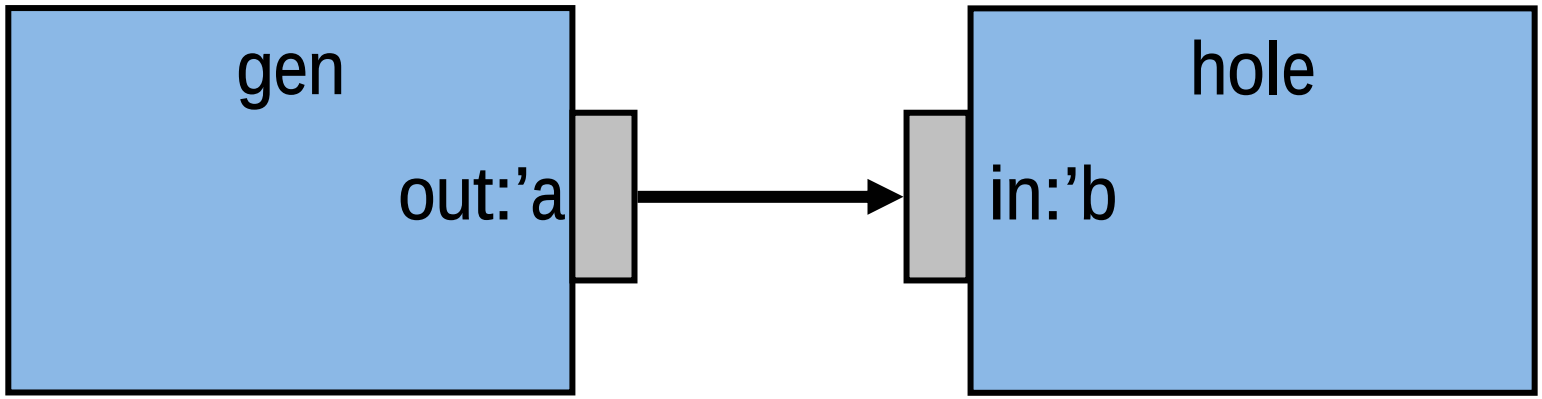
Polymorphism

Type Inference



- Source and sink modules are polymorphic
- Type inference cannot resolve polymorphism!

Type Constraints



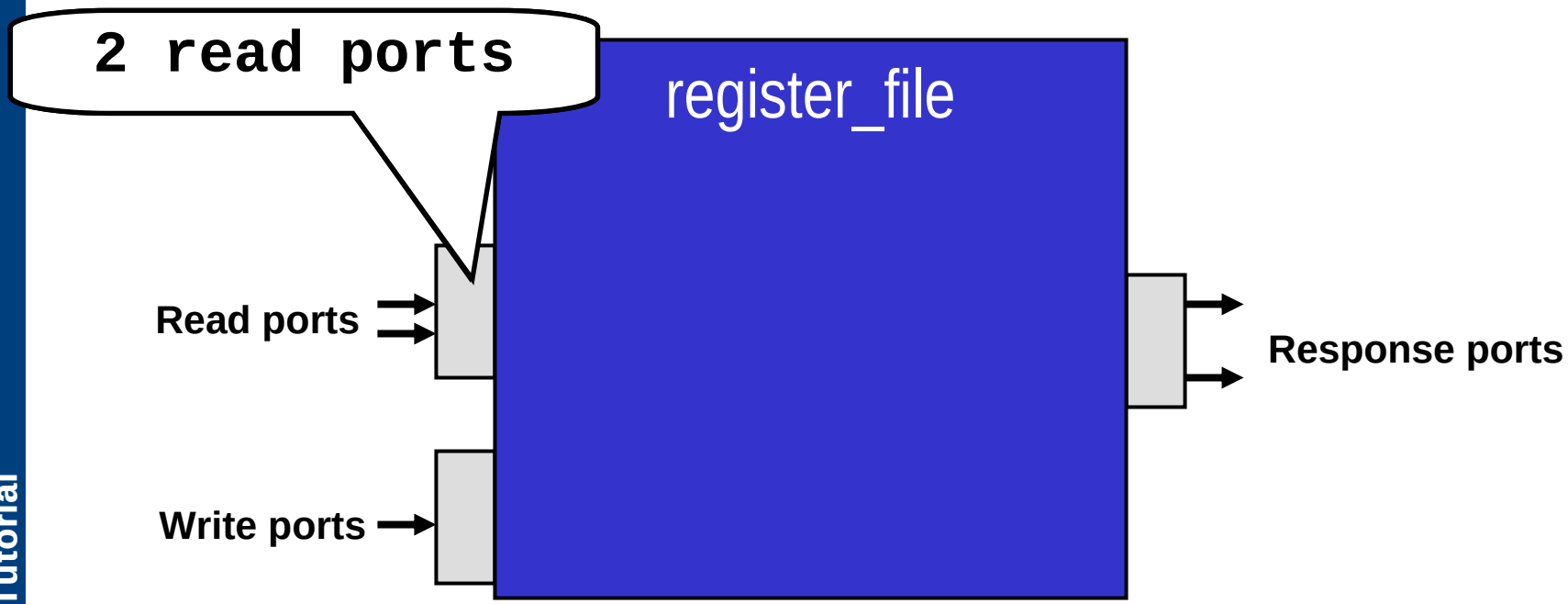
- `'a=int, 'b=int`

```
using corelib;

instance gen:source;
instance hole:sink;

gen.out ->[int] hole.in;
```

User can constrain types

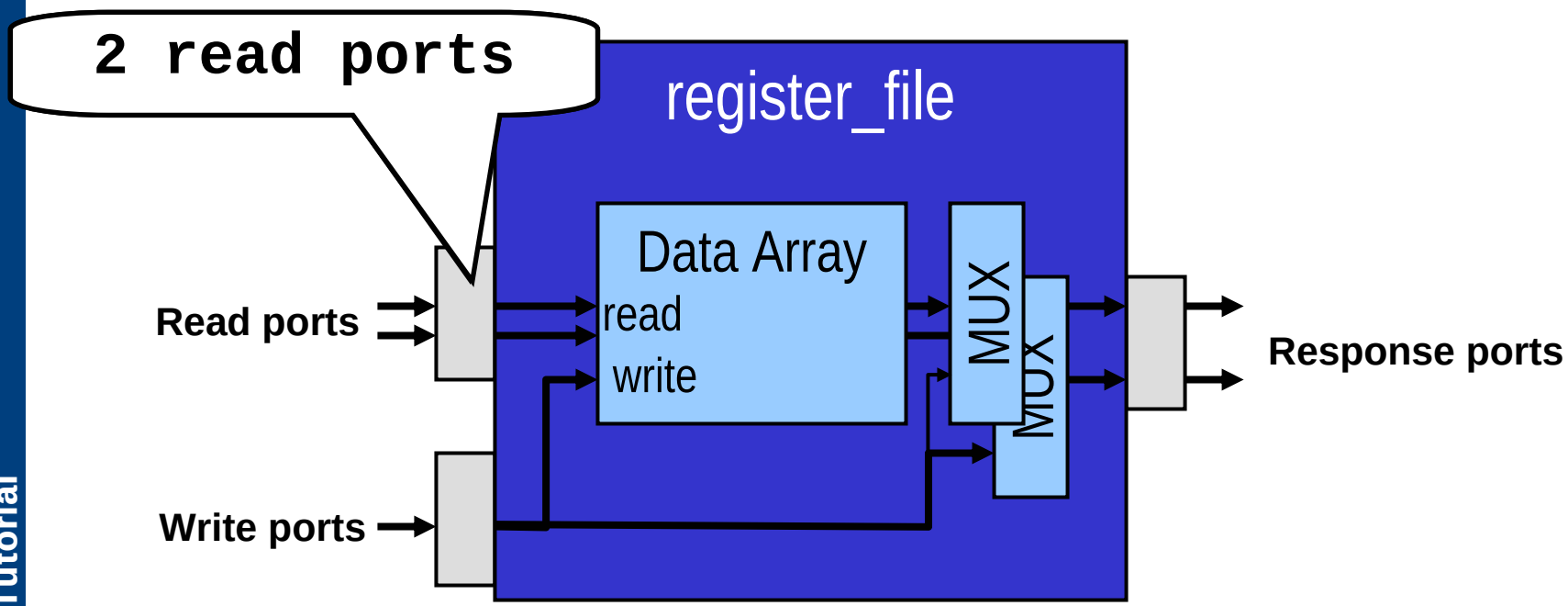
Flexible Structure

Scalable Port-Widths



- Flexible interfaces needed for reuse
  - e.g., control the request width result width
- Examples
  - Number of read ports on register files and memories
  - Sizing of crossbars and arbiters
  - Branch prediction requests

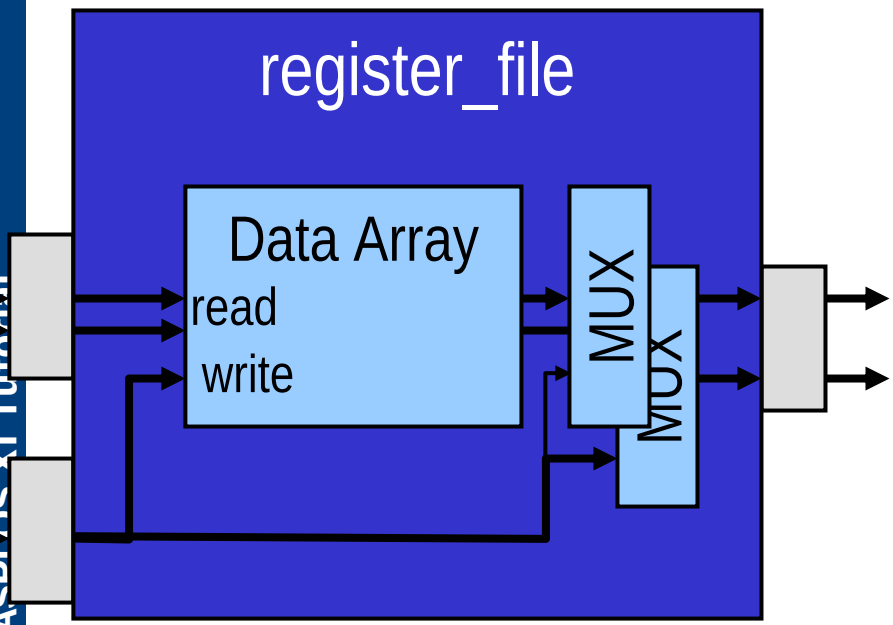
Parametric Customization of Structure



- Different levels model refinement require different number of ports
- Variation in ports requires varying structure
  - One register read port requires one MUX
  - Two register read ports requires two MUXes

Parametric Customization of Structure

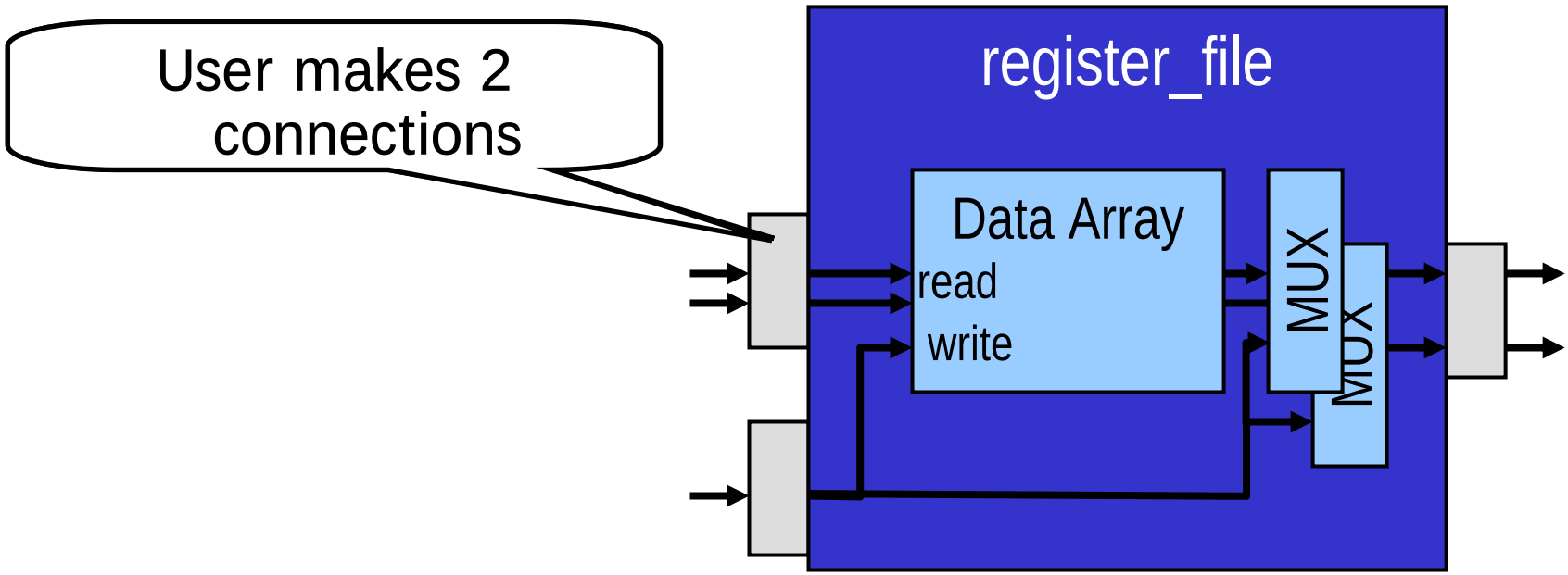
```
num_reads = 2;
```




```
module register_file {
parameter num_reads:int;

  inport read:read_req;
  inport write:write_req;

  instance data_array:…;
  instance muxes:
           mux[num_reads];
  for(i=0;i<num_reads;i++){
    data_array.out[i] ->
       muxes[i].in[0];
  }
  …
};
```

- Flexible interface add parameterization overhead
  - Our Itanium 2 model needs 523 interface sizing parameters

Lowering Overhead with Use-based Specialization

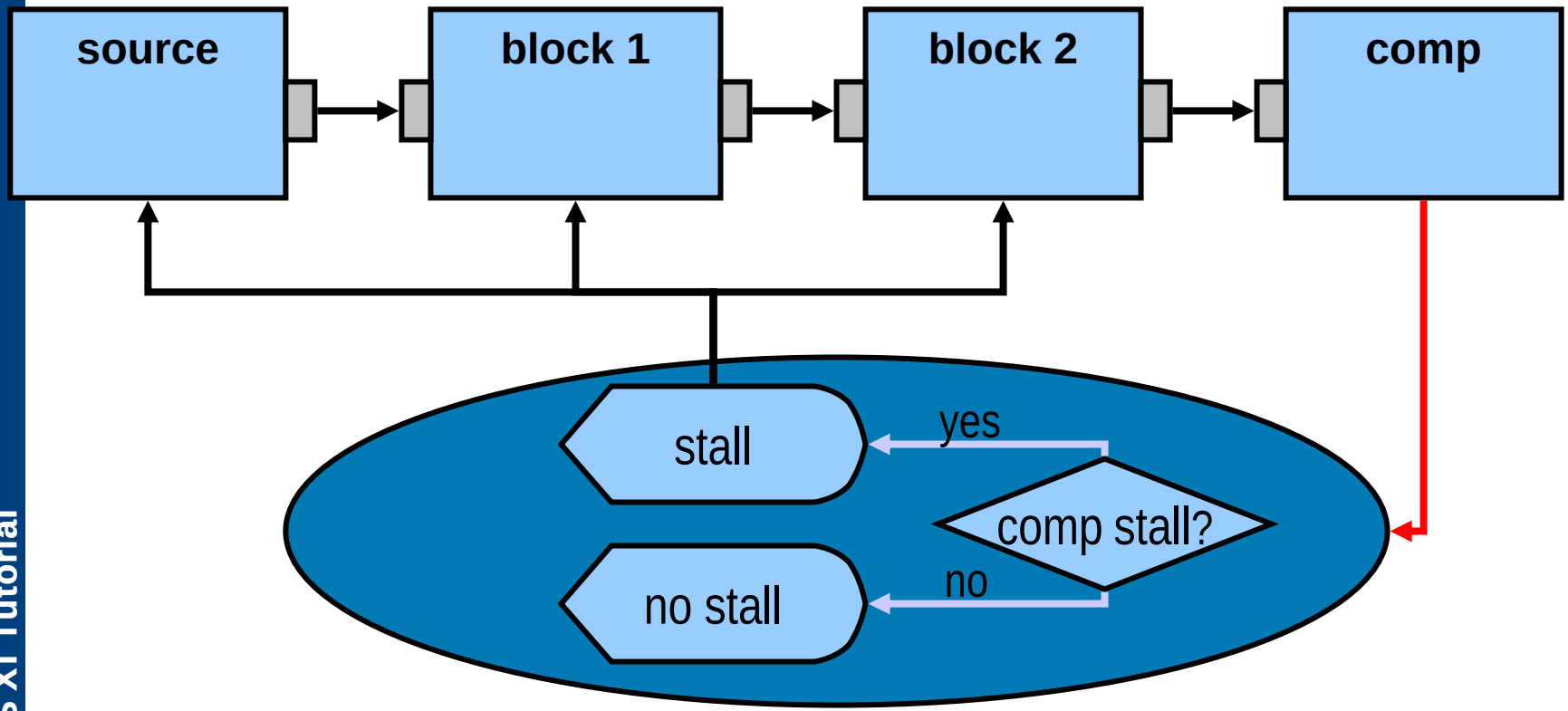


- Infer parameters from usage (i.e. use-based specialization)
- Other customizations based on usage
  - Types – if auxillary data ports connected, output type is a **`struct`**
  - Semantics – If branch target port is connected a BTB is instantiated
- Eliminates 523 interface size parameters for I2 model

Torus Live Demo

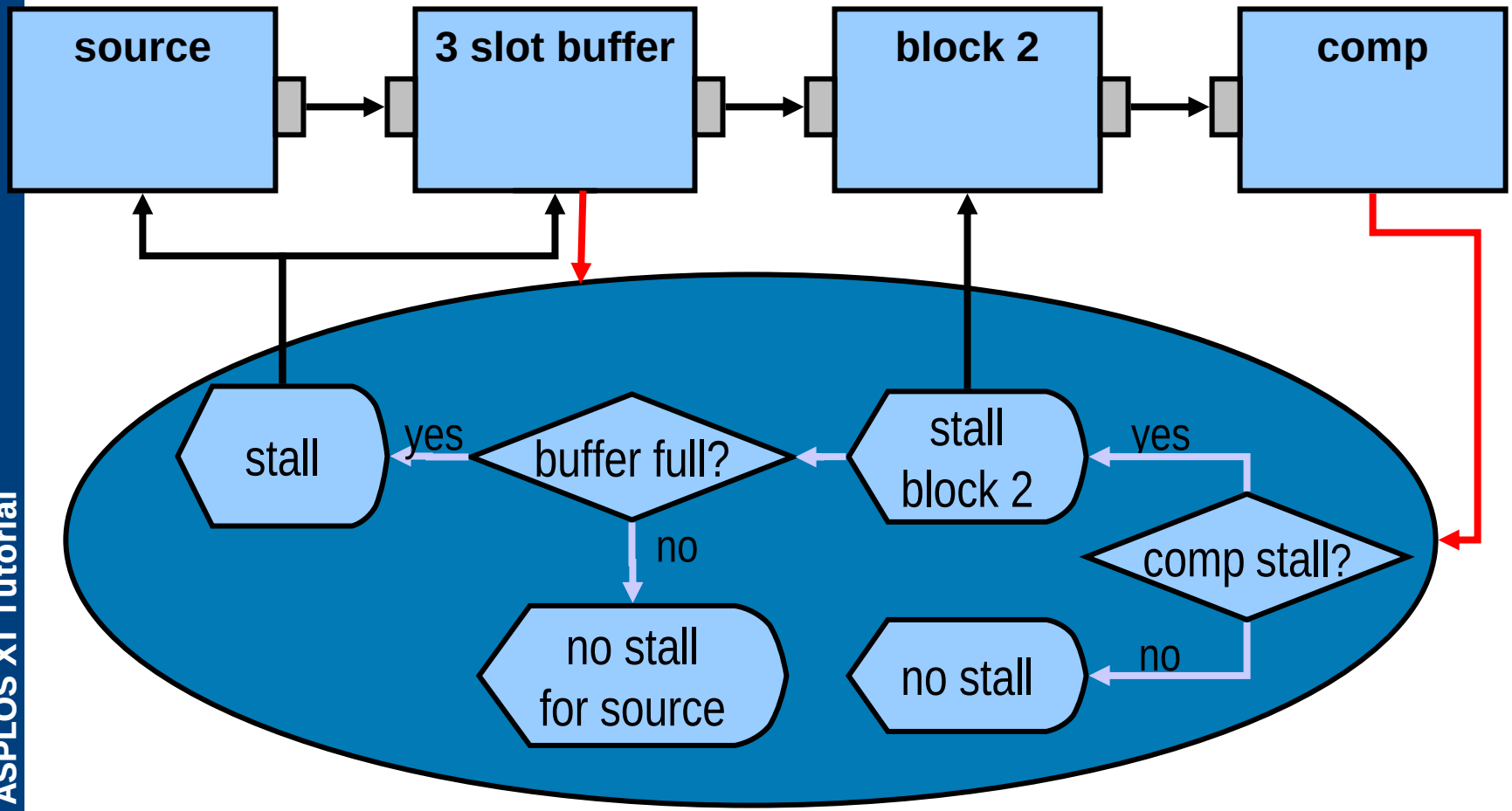
Control in LSE

Timing Control Example



- Timing control handles stalling
- Timing control is logically centralized
  - Controller has global knowledge

More Complex Timing Control

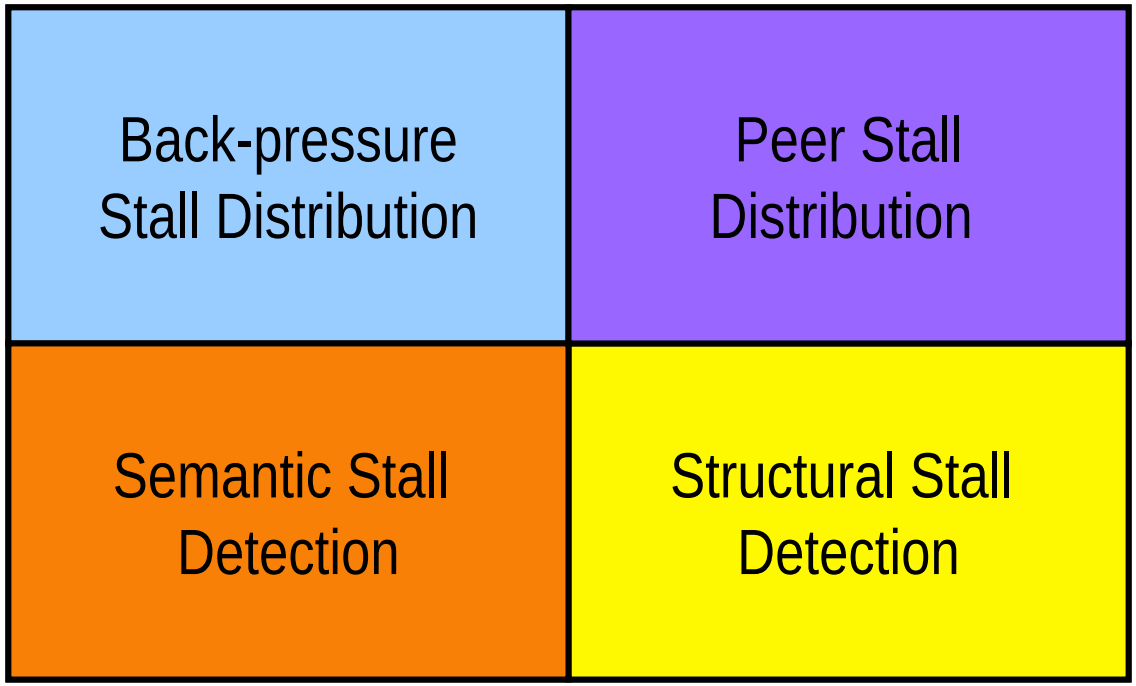


- Even simple data path changes require updating the controller
- Controller cannot be reused!

Timing Control and Existing Modeling Systems

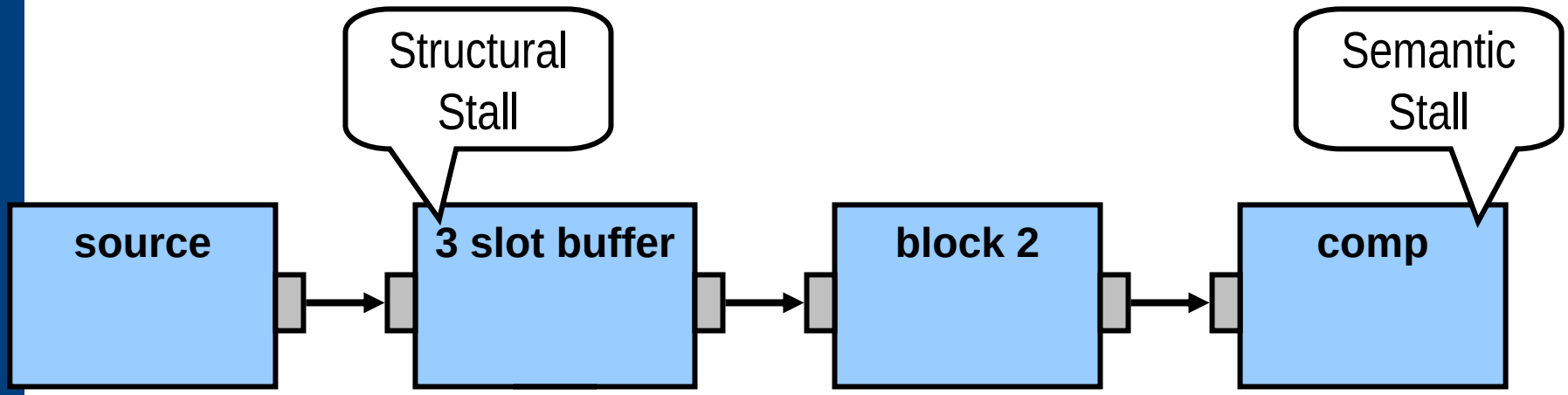
- Existing work treats timing-control as global entity
- Control neutrality
  - SystemC, Objective VHDL, UPFAST, HASE, etc.
  - Approaches focus on other problems, not timing-control
- Specification of global timing controller
  - Generality versus complexity tradeoff
  - Template-based
    - LISA [Pees '99], RADL [Siska '98]
    - Very limited architecture class
  - Alternative representations
    - Expression [Mishra '01], MADL [Qin '02]
    - Generality vs. complexity
- Modularize control instead

The Components of Timing Control



- Stall detection – when to stall
  - Structural stall conditions
  - Semantic stall conditions
- Stall distribution – what to stall
  - Backpressure stall distribution
  - Peer stall distribution

Stall Detection

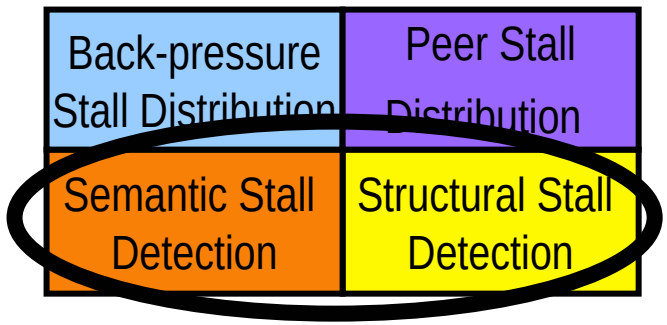


Semantic stalls

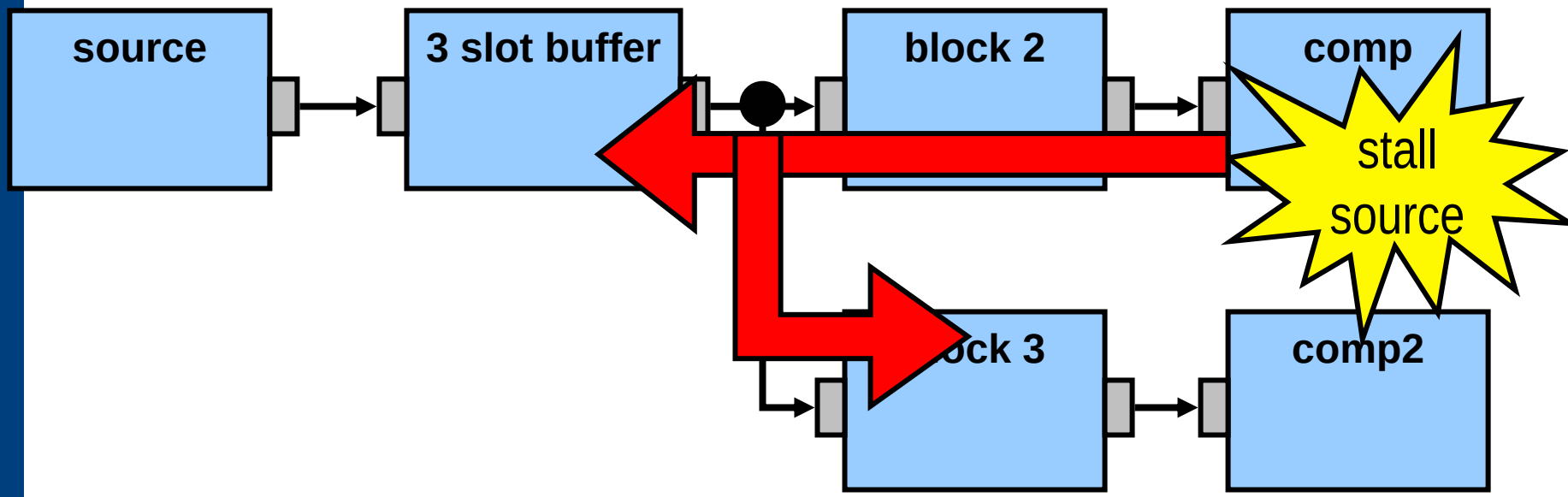
- Stall condition varies as semantics change
- Data hazards, control hazards, etc.

Structural stalls –

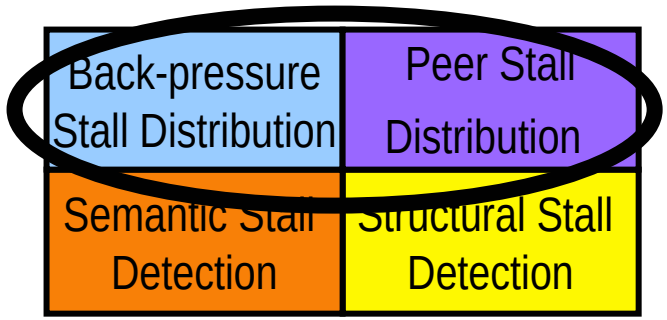
- Stall condition invariant across different semantics
- No buffer slots, bus arbitration loss, etc.
- Should be reusable!



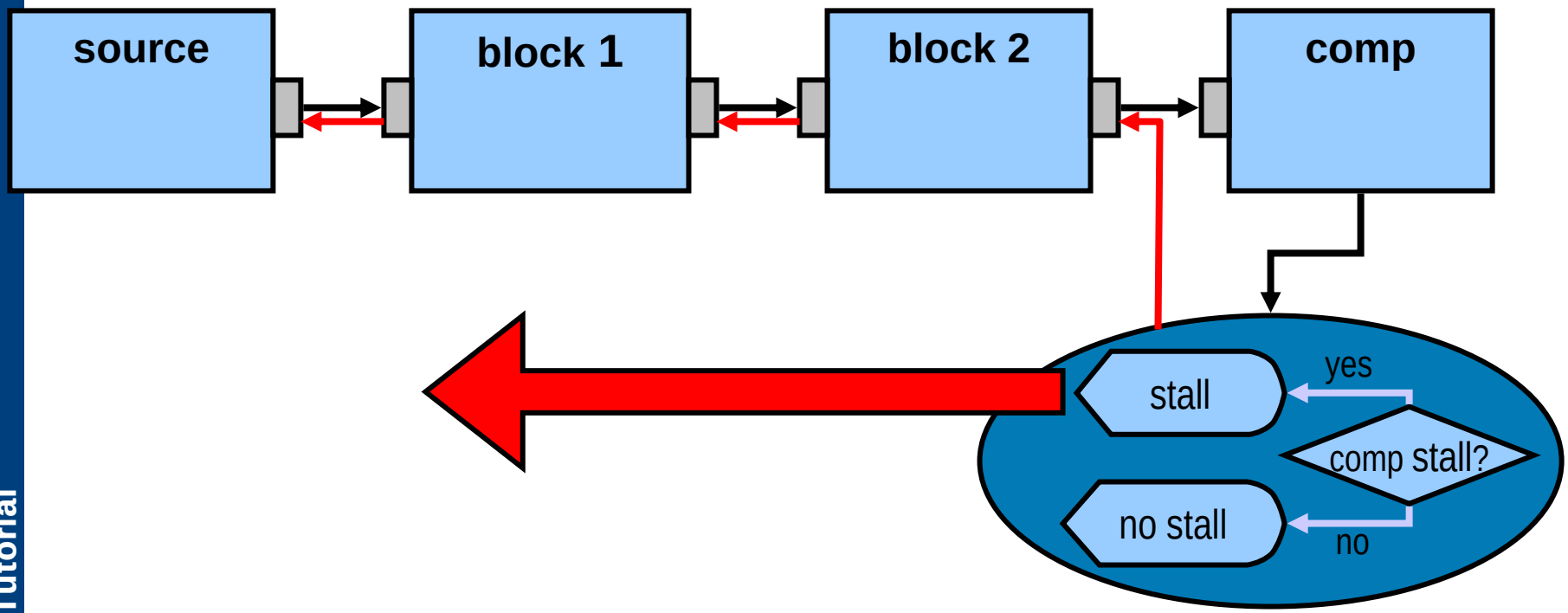
Stall Distribution



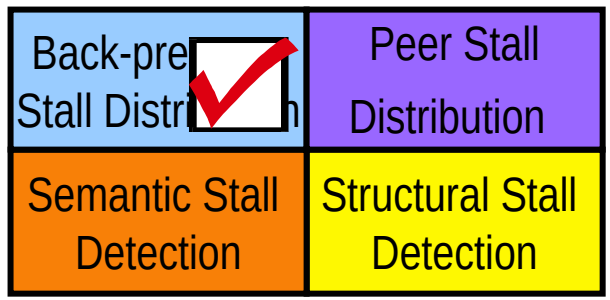
- Stalls propagate along the datapath
- Back pressure
  - Stall earlier blocks in the pipeline
  - Follows opposite direction of datapath
- Coordination
  - Stall peers in the pipeline
  - Usually follows datapath at fanout nodes



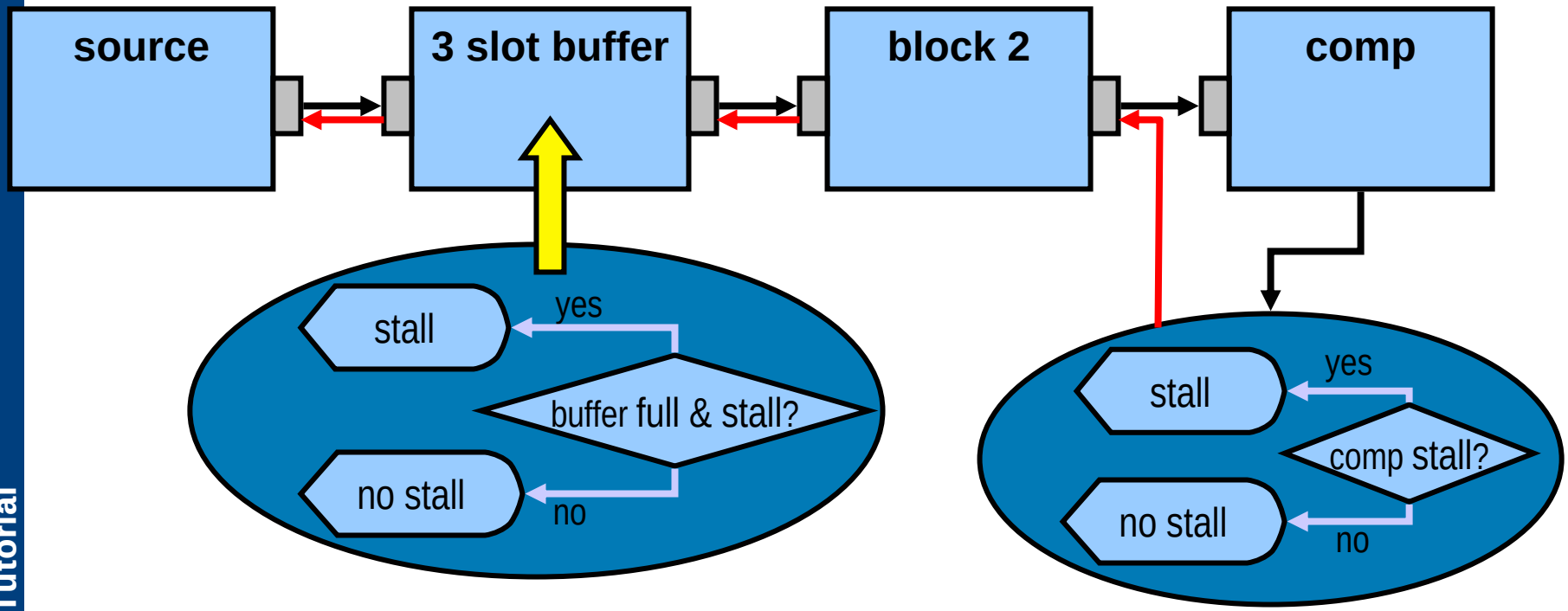
Modularizing Backpressure Stall Distribution



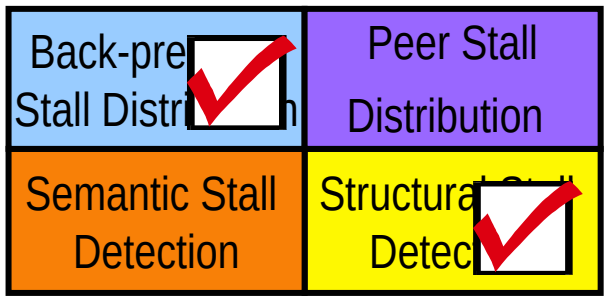
- Reverse control signal for backpressure stalls



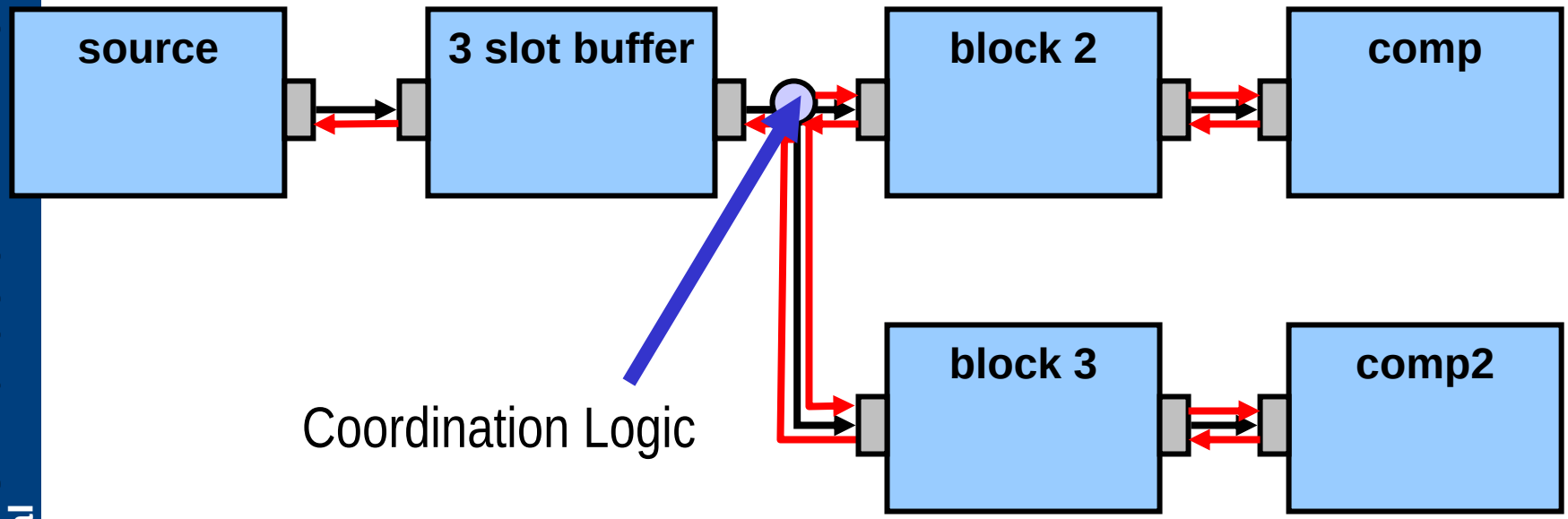
Modularizing Structural Stall Detection



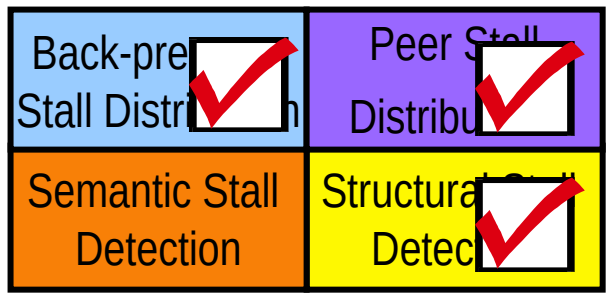
- Structural stalls encapsulated in reusable components



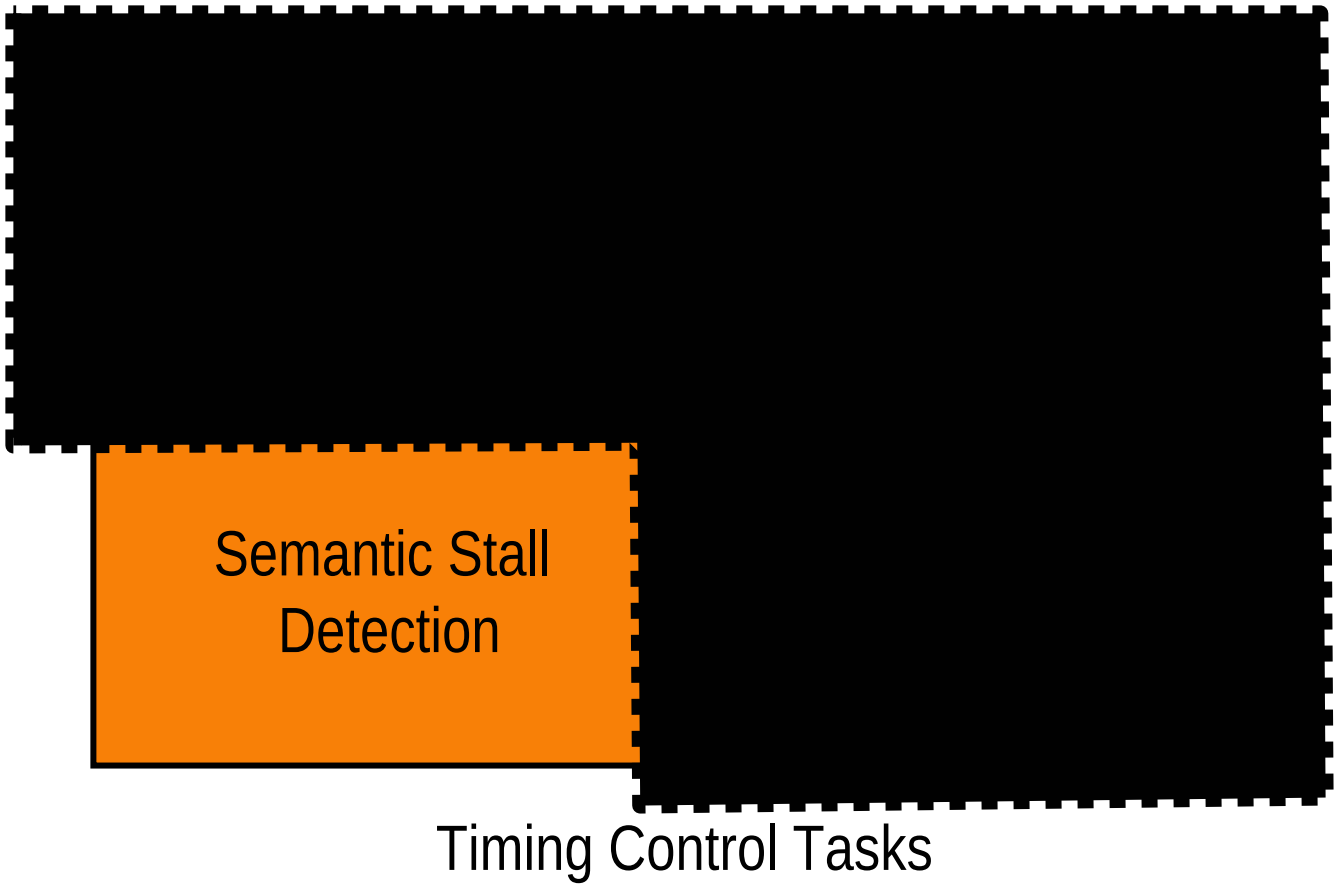
Modularizing Peer Stall Distribution and Coordination



- Forward control signal handles peer stalls
- Coordination controlled at fanout
  - Reasonable default semantics for almost all components
  - User over-ridable



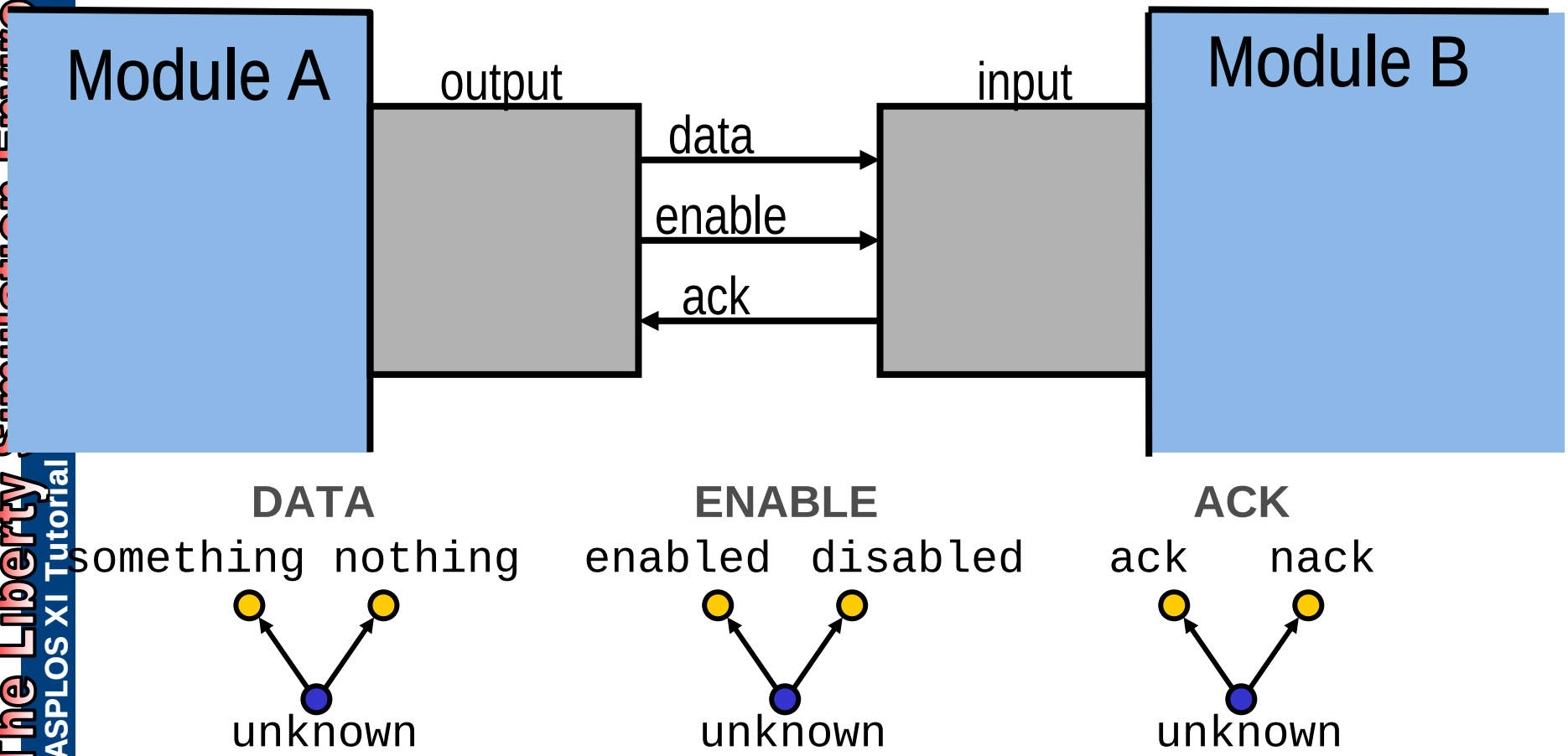
Timing Control Modularization Summary



- Control abstraction makes 3 of 4 portions reusable
- Other approaches good at semantic stalls
  - Expression, MADL, etc. can be leveraged!

Control Signals

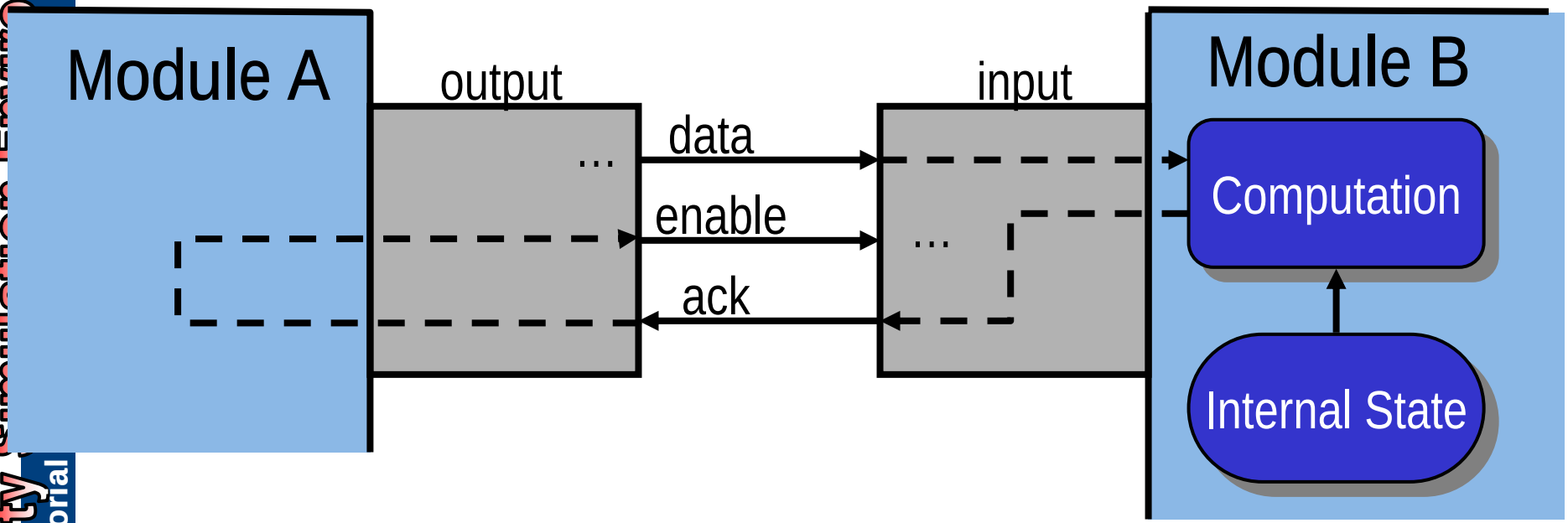
3 Signal Values



- Transition from unknown to *one* known value per cycle

Control Signals

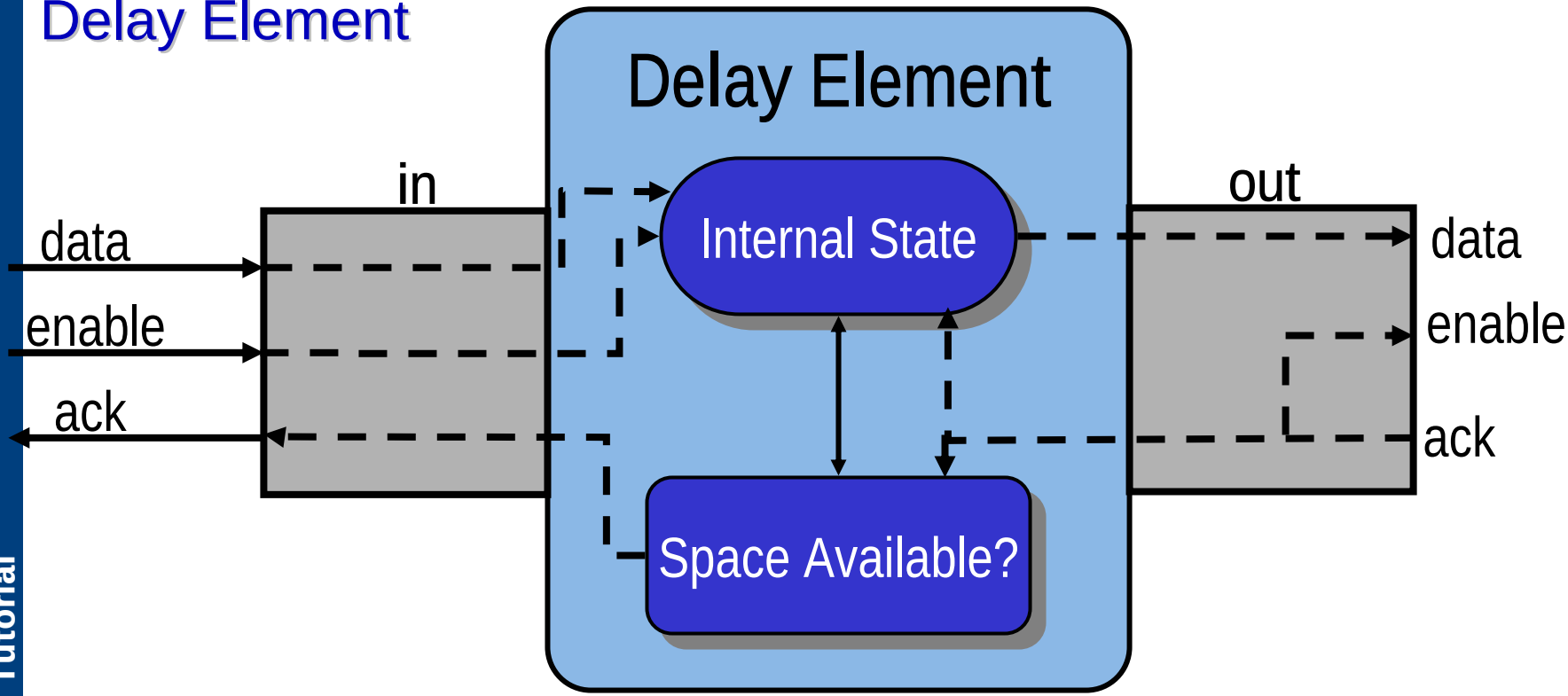
3 Signal Semantics



- Module A sends data (unknown -> something | nothing)
- Module B receives data and acknowledges
  - unknown -> ack
- Module A enables based on acknowledge
  - unknown -> enabled

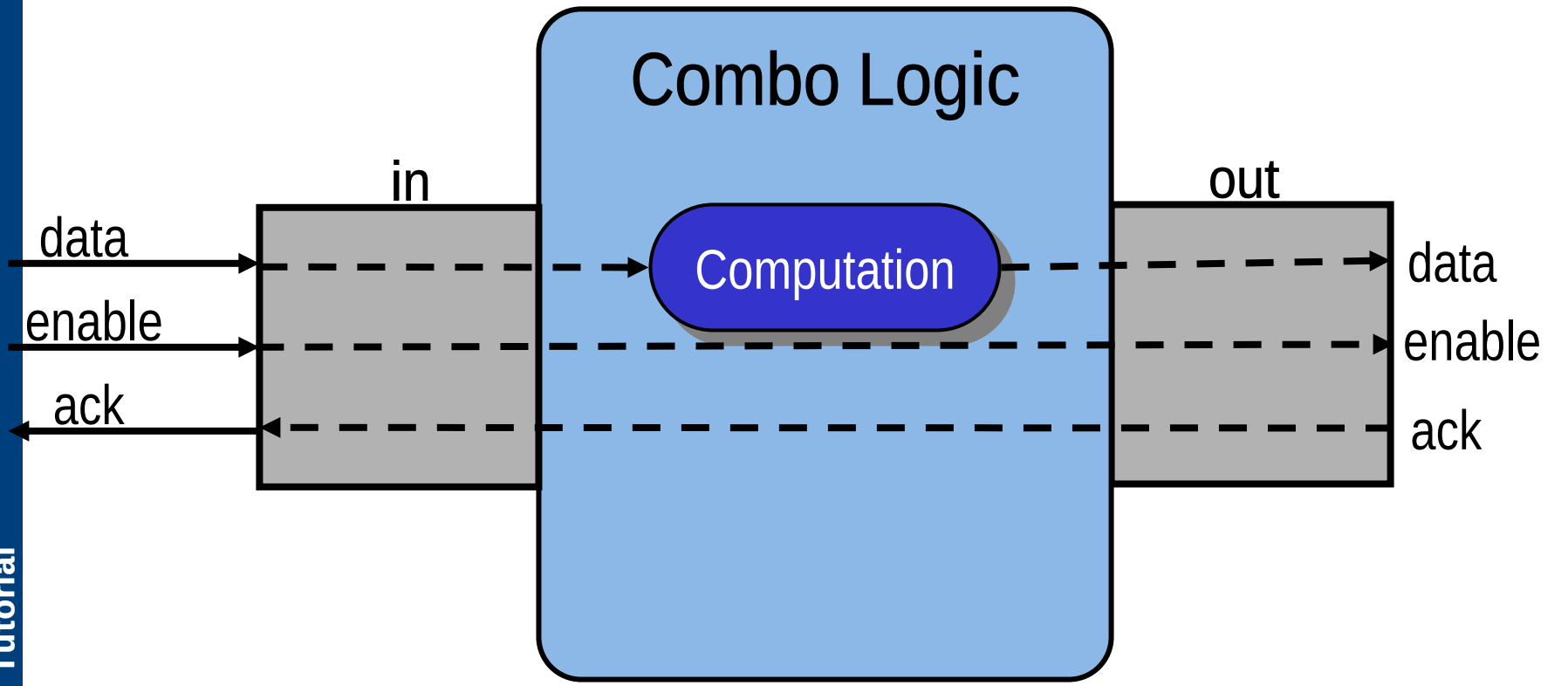
Control Signals

Delay Element



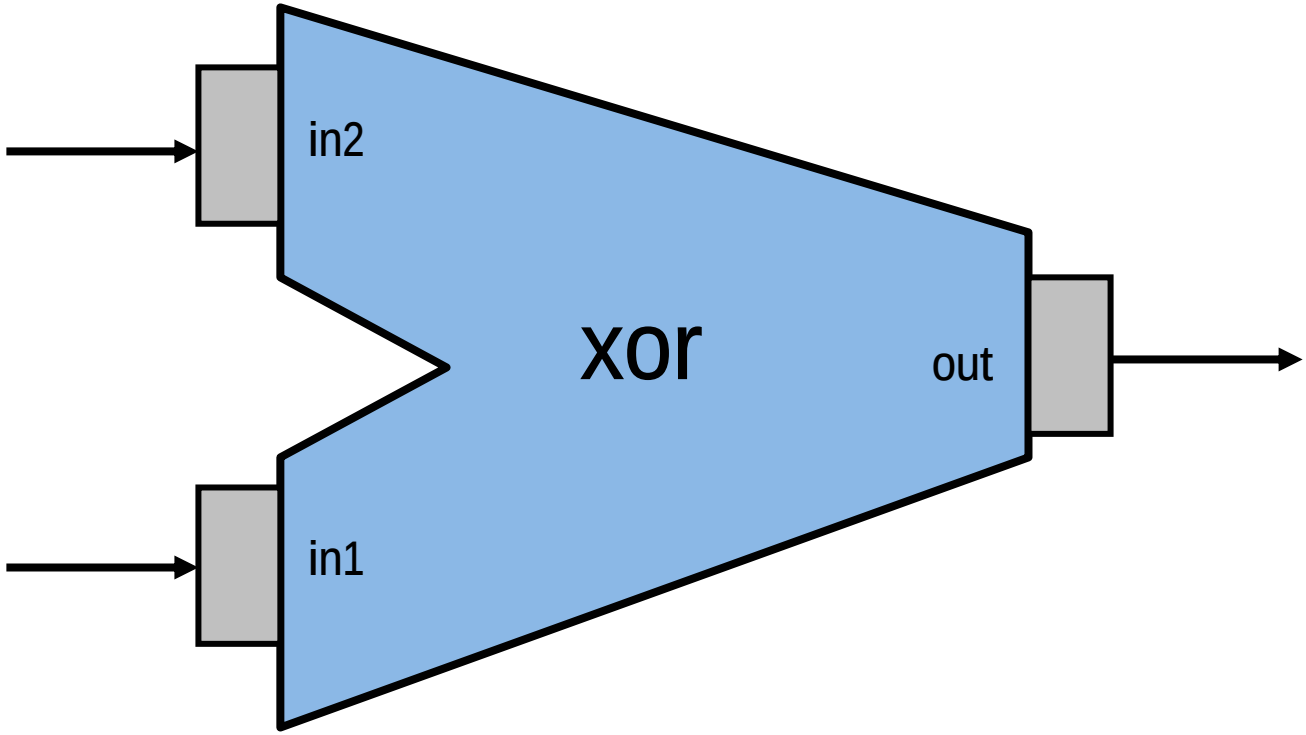
- If space is available
  - Send ack
  - If input enabled, update state at the end of cycle
- Otherwise
  - Send nack

Combinational Control Signals



- Process input data and generate new data
- Pass enable and ack straight through

Combinational Control Signals



For multiple inputs

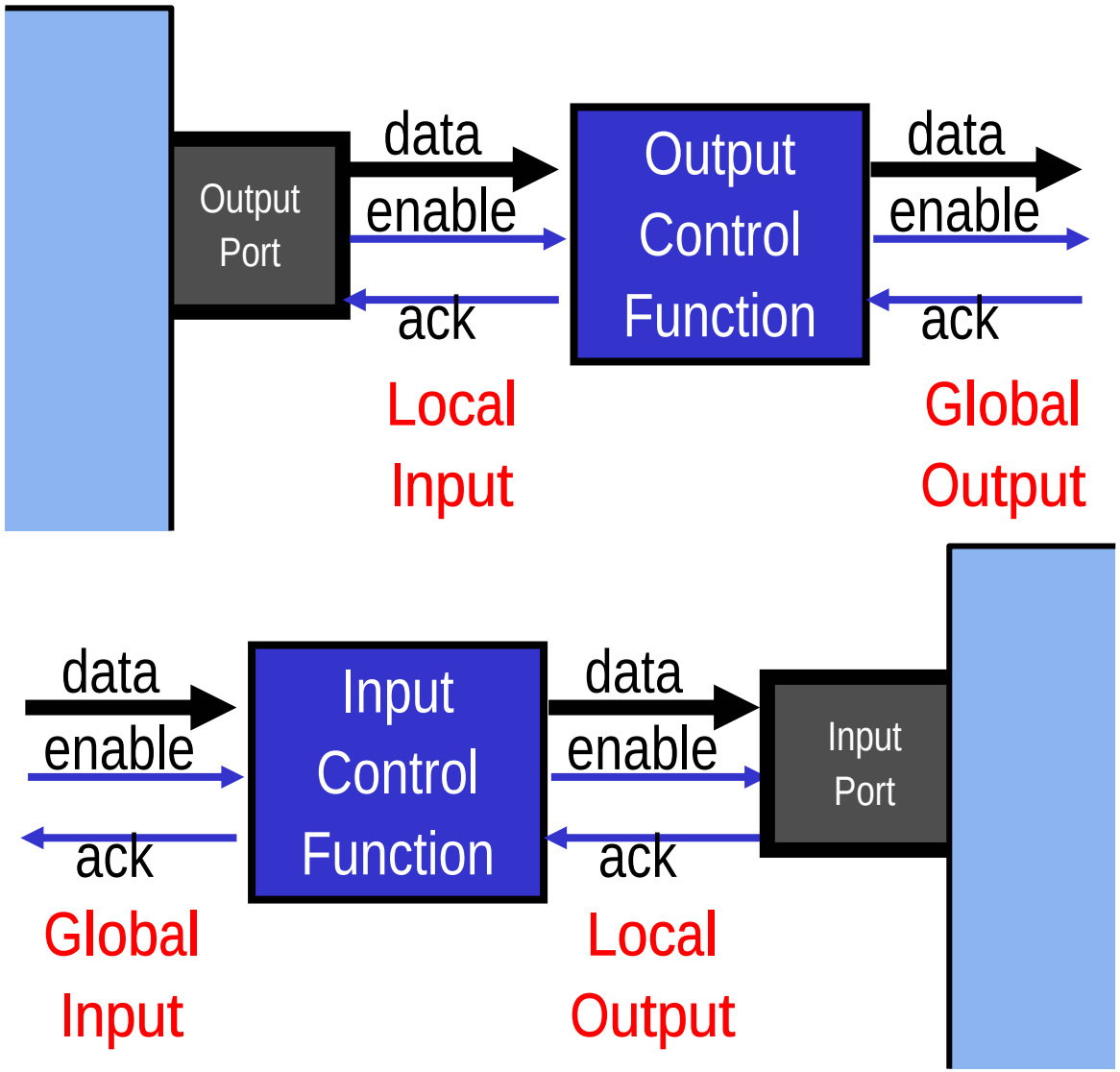
- Combine enable signals
- Fan out ack signals

Live Demo
Putting it all together - Pipeline Stall Control

Live Demo
Putting it all together – Stalls in the Torus

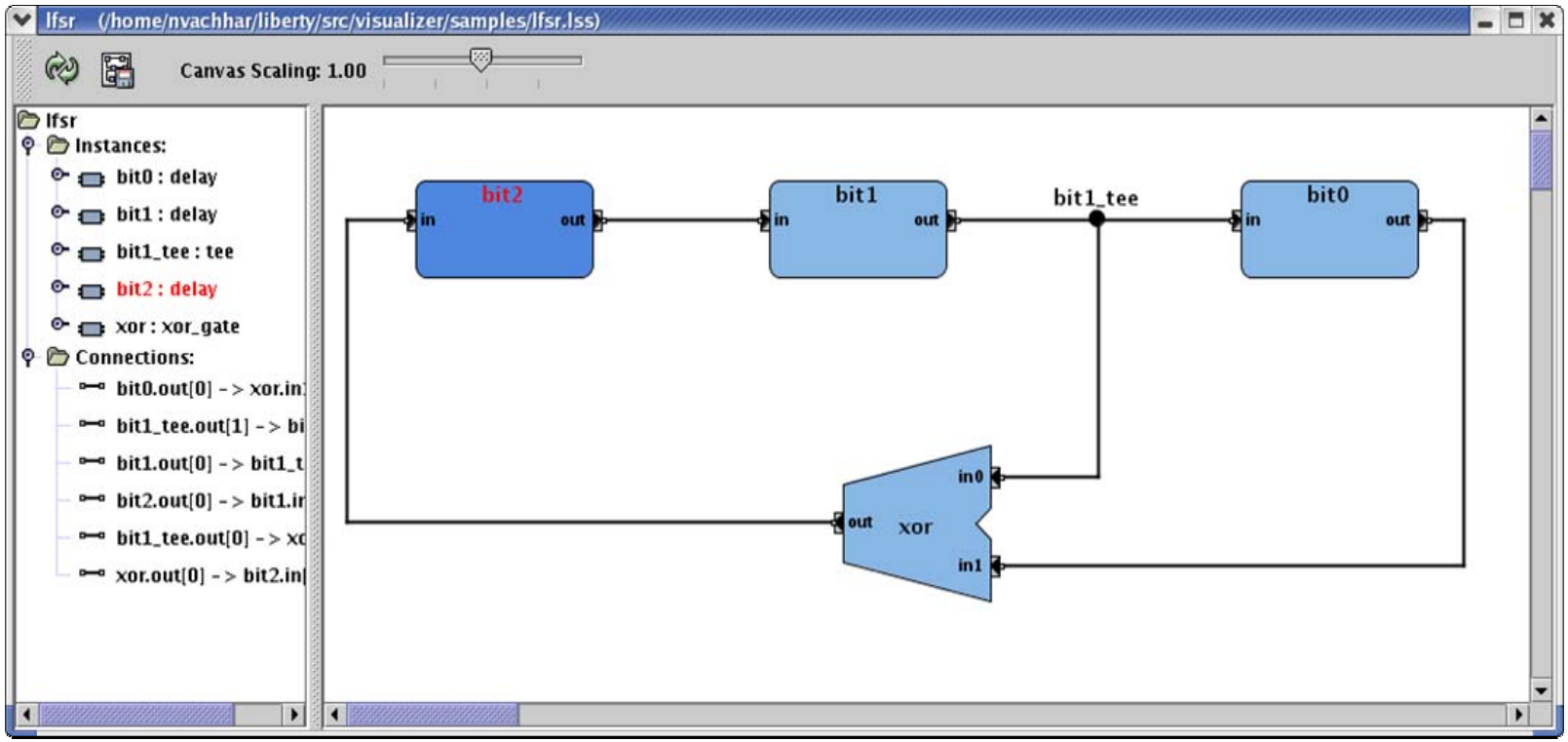
Customizing Control

Control Functions



Control Functions

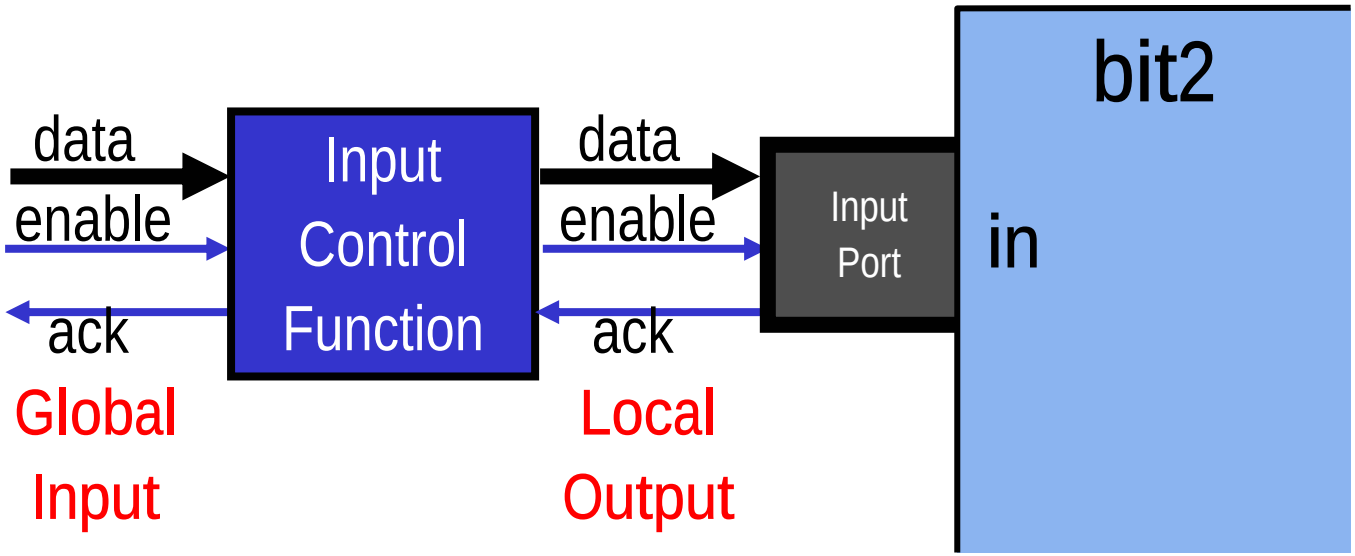
LFSR Control



- Desired Control
  - Every bit updates every cycle

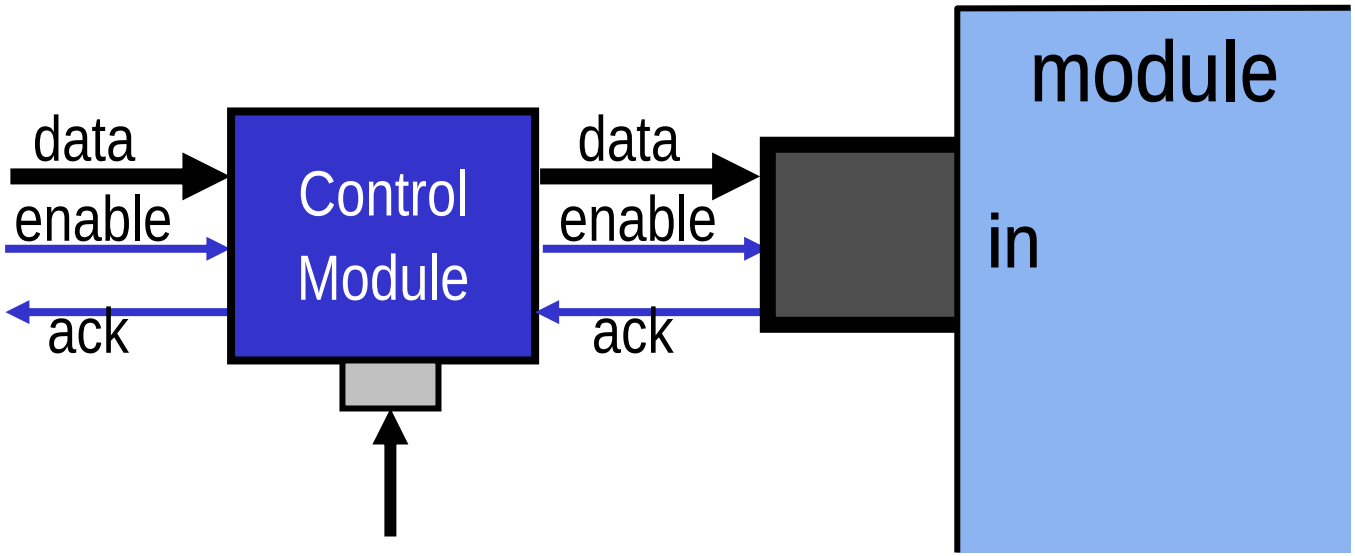
Control Functions

LFSR Custom Control




```
bit2.in.control = <<<
  return LSE_signal_extract_data(istatus) |
         LSE_signal_enabled |
         LSE_signal_ack;
>>>;
```

Structural Control



- Control Function was like a small module
- Can make this explicit
  - Add extra inputs
  - Build using reusable concurrently executing components
  - e.g. gate module in corelib

Control Review

- Default Control
  - Corresponds to back-pressure
  - Makes reusing components easy in common case
- Control Functions
  - Customize control locally
  - Simple, easy to specify
- Explicit Structural Control
  - When all else fails, use explicit control structure

End of Part 1

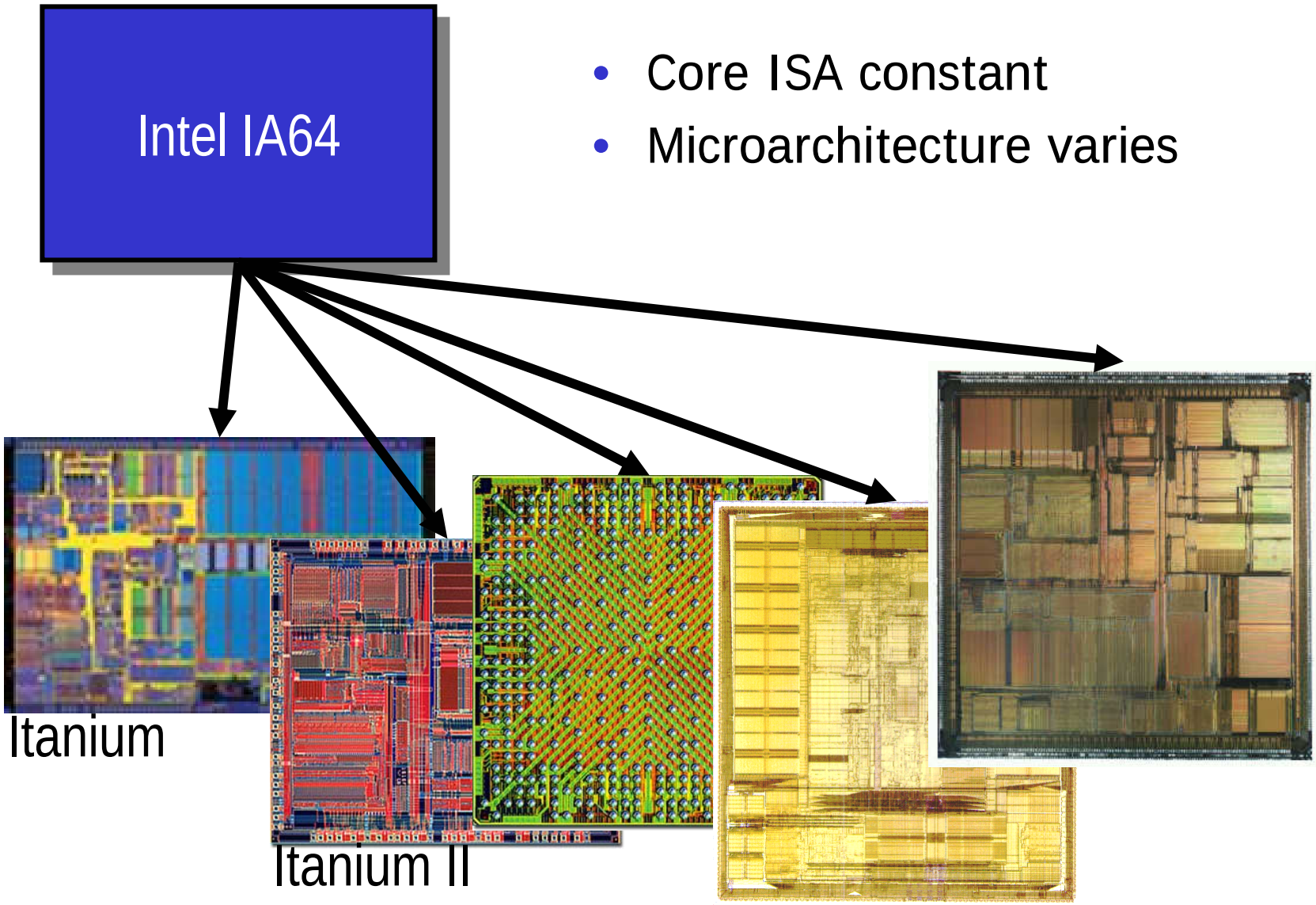
30 minute break

Building Processor Models

Part 2

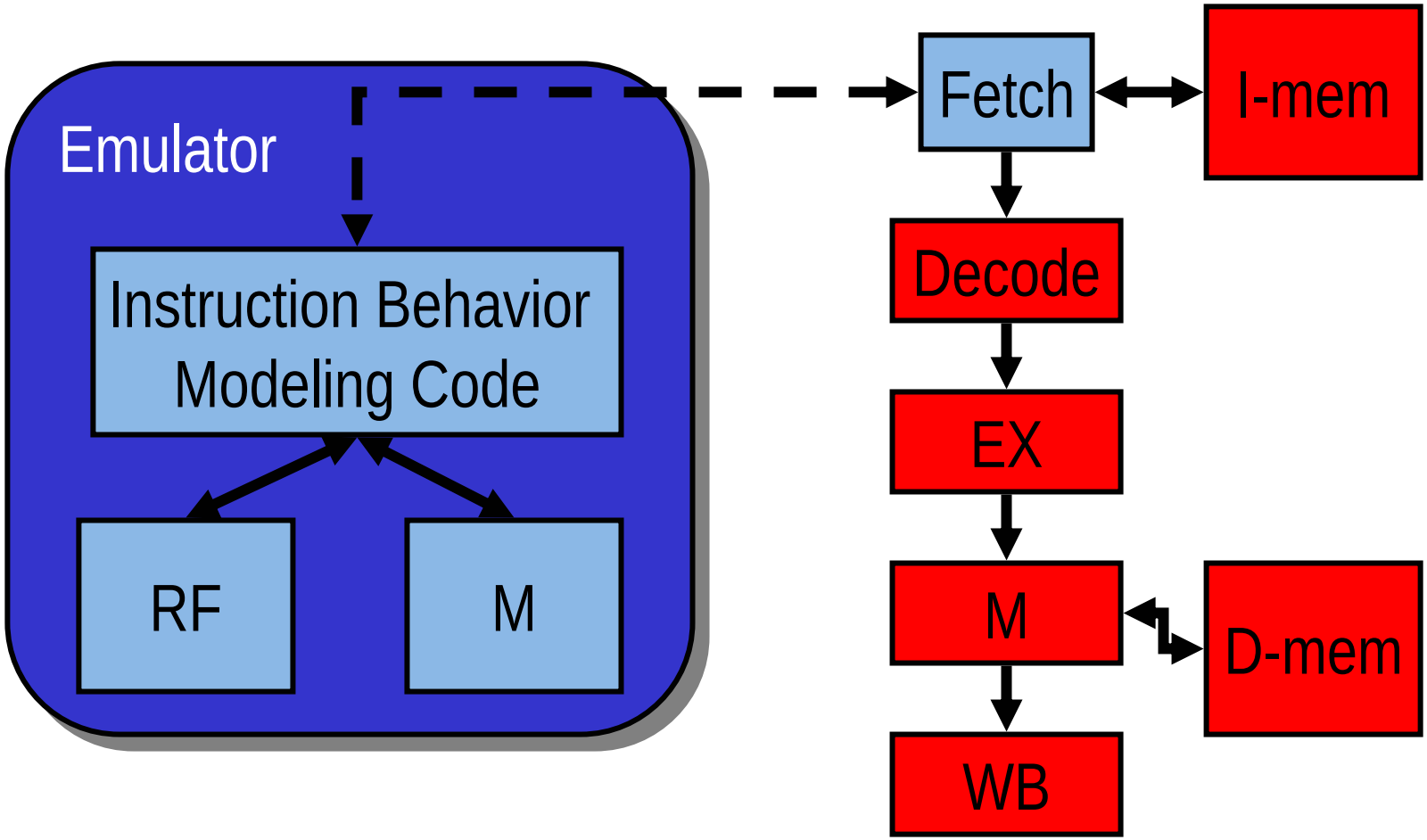
DLX Config

Microarchitecture and ISA

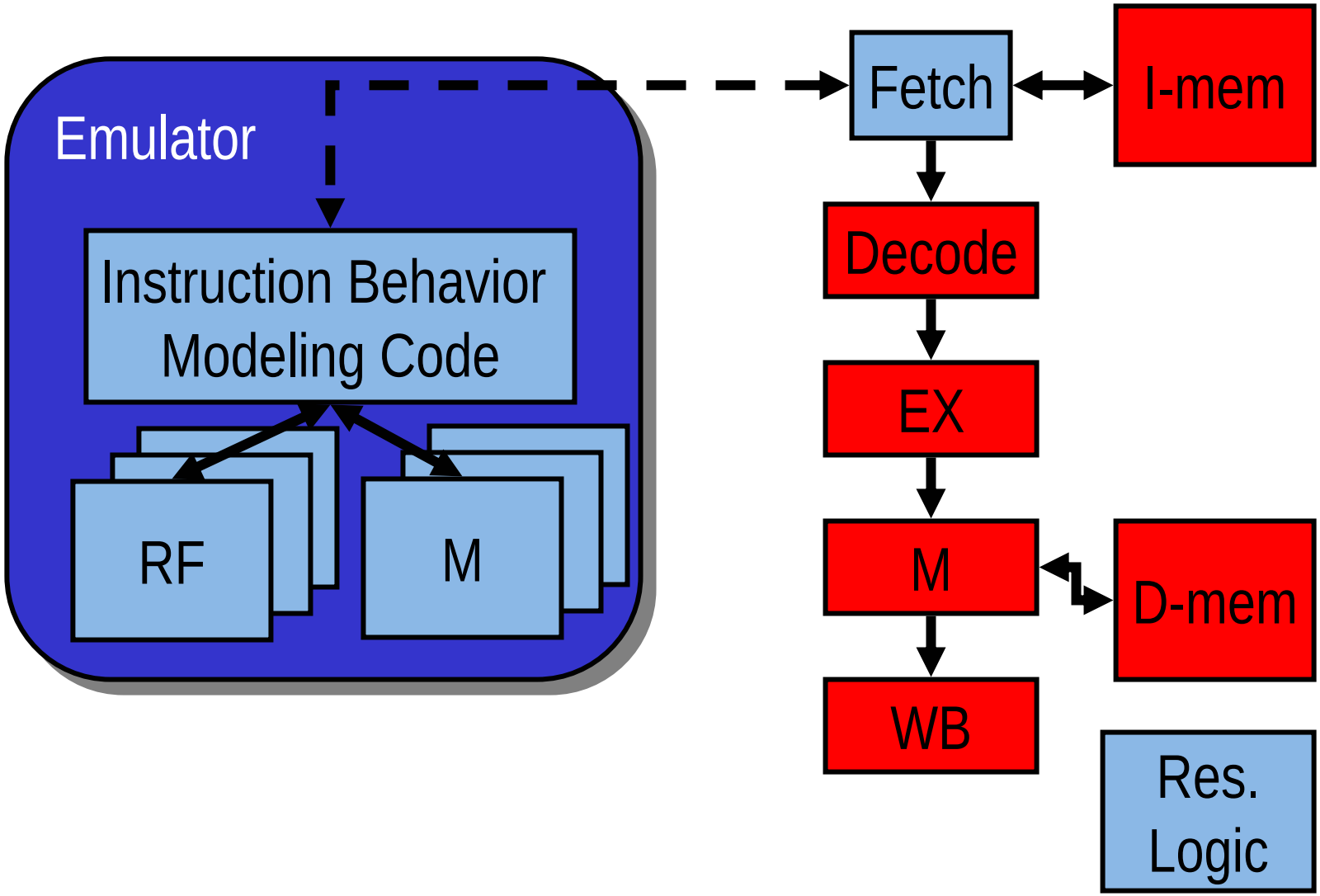


- Core ISA constant
- Microarchitecture varies

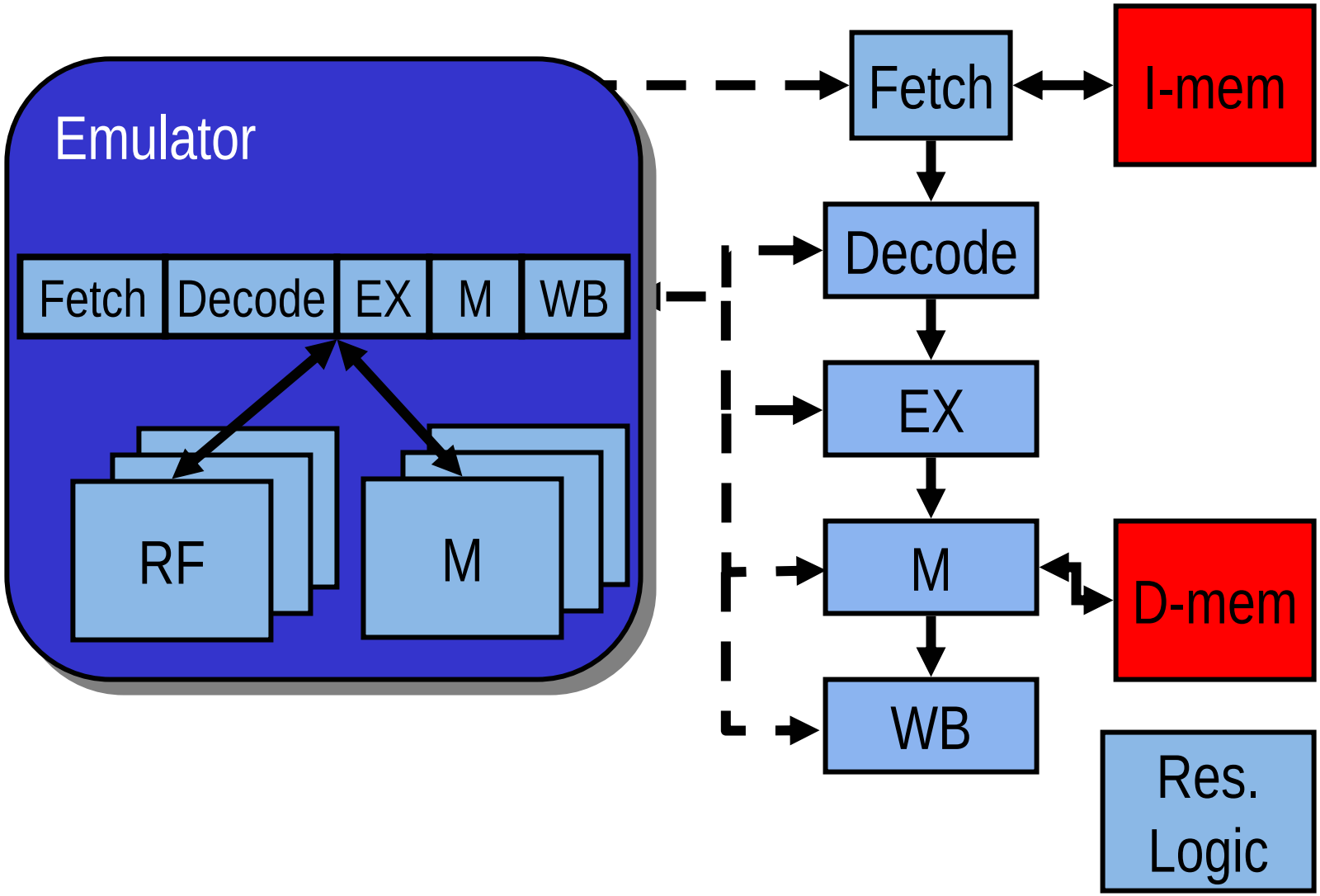
Bulk Execution



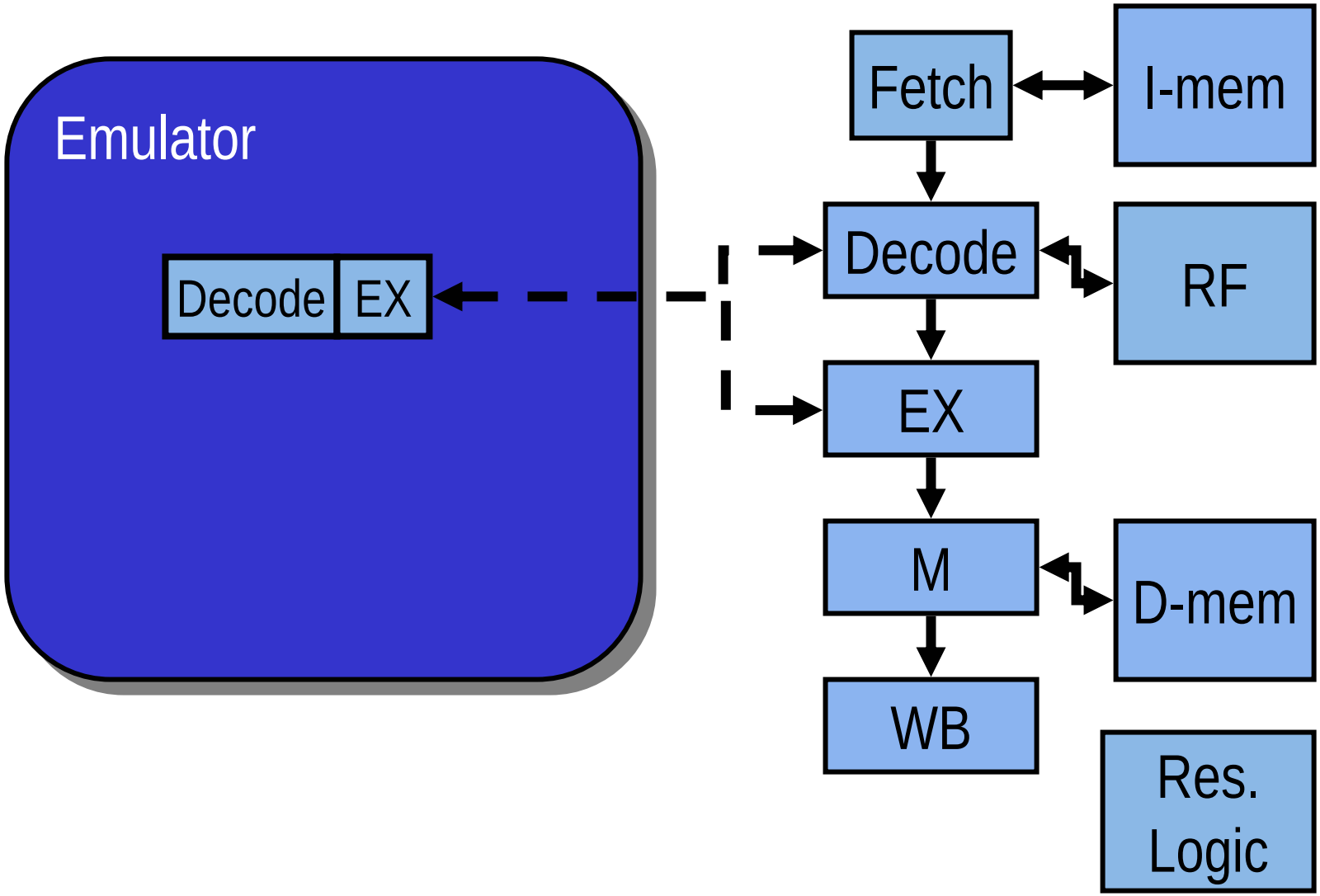
Bulk Execution w/ Rollback



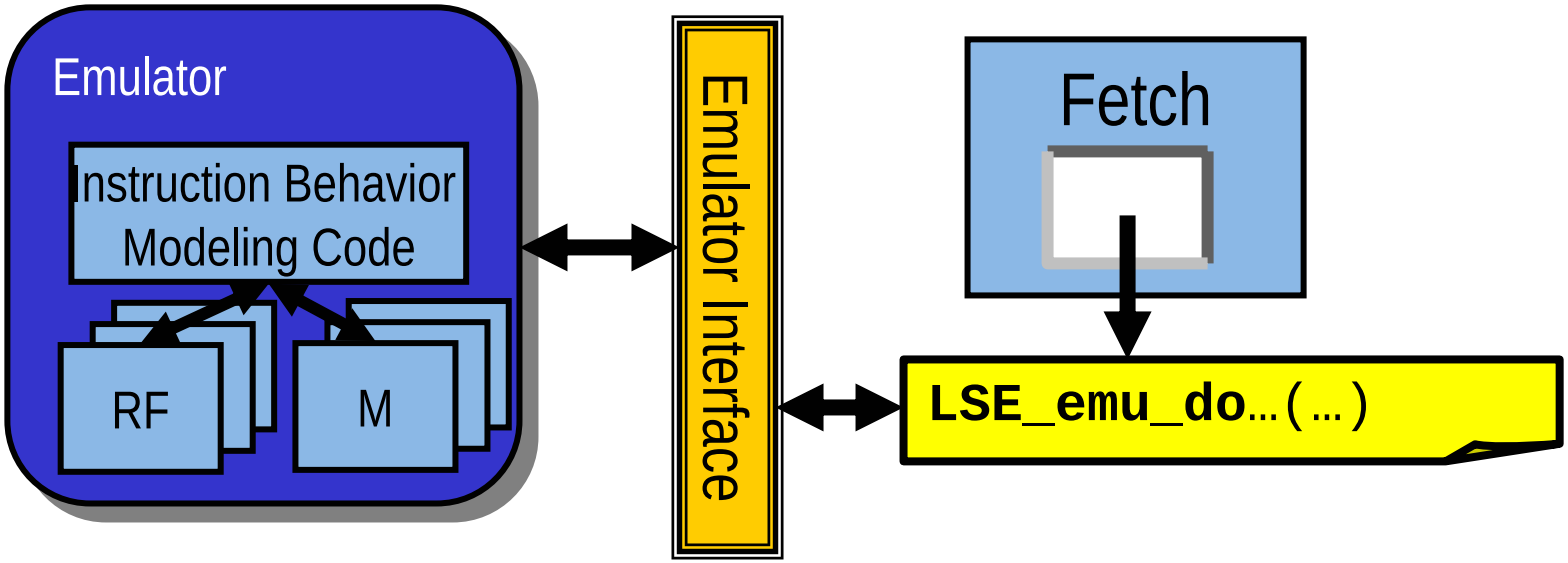
Full Callback



Microarchitecture Model Maintains ISA State



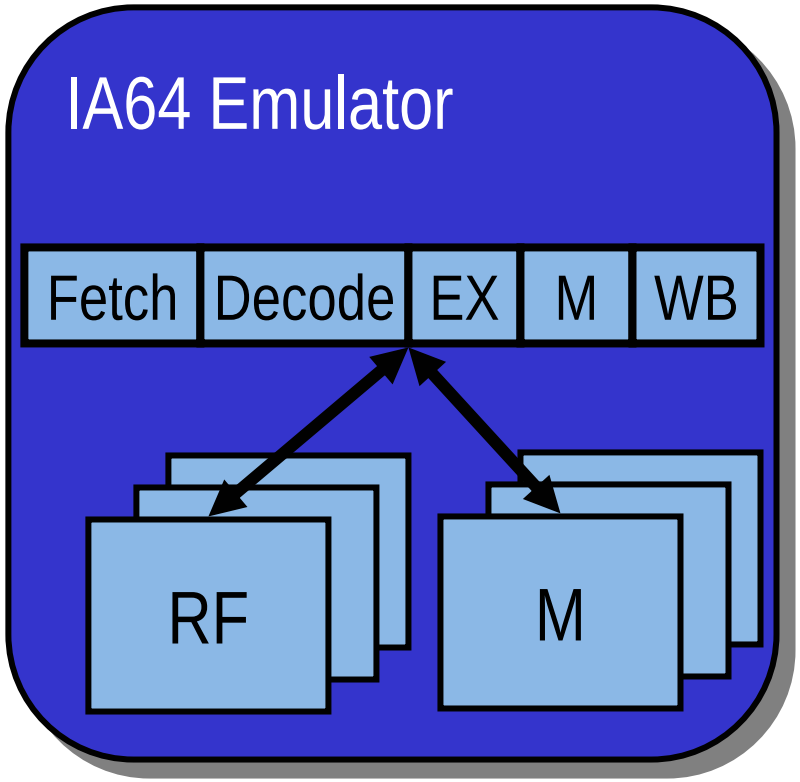
Emulation in LSE



- LSE Supports Abstraction of ISA functionality
  - via the *emulator* interface
- Microarchitecture model invokes functions in ISA model to implement instruction behavior
- Emulator interface is flexible
  - As simple as bulk emulation at fetch
  - Detailed enough for all data to be managed in μarch model

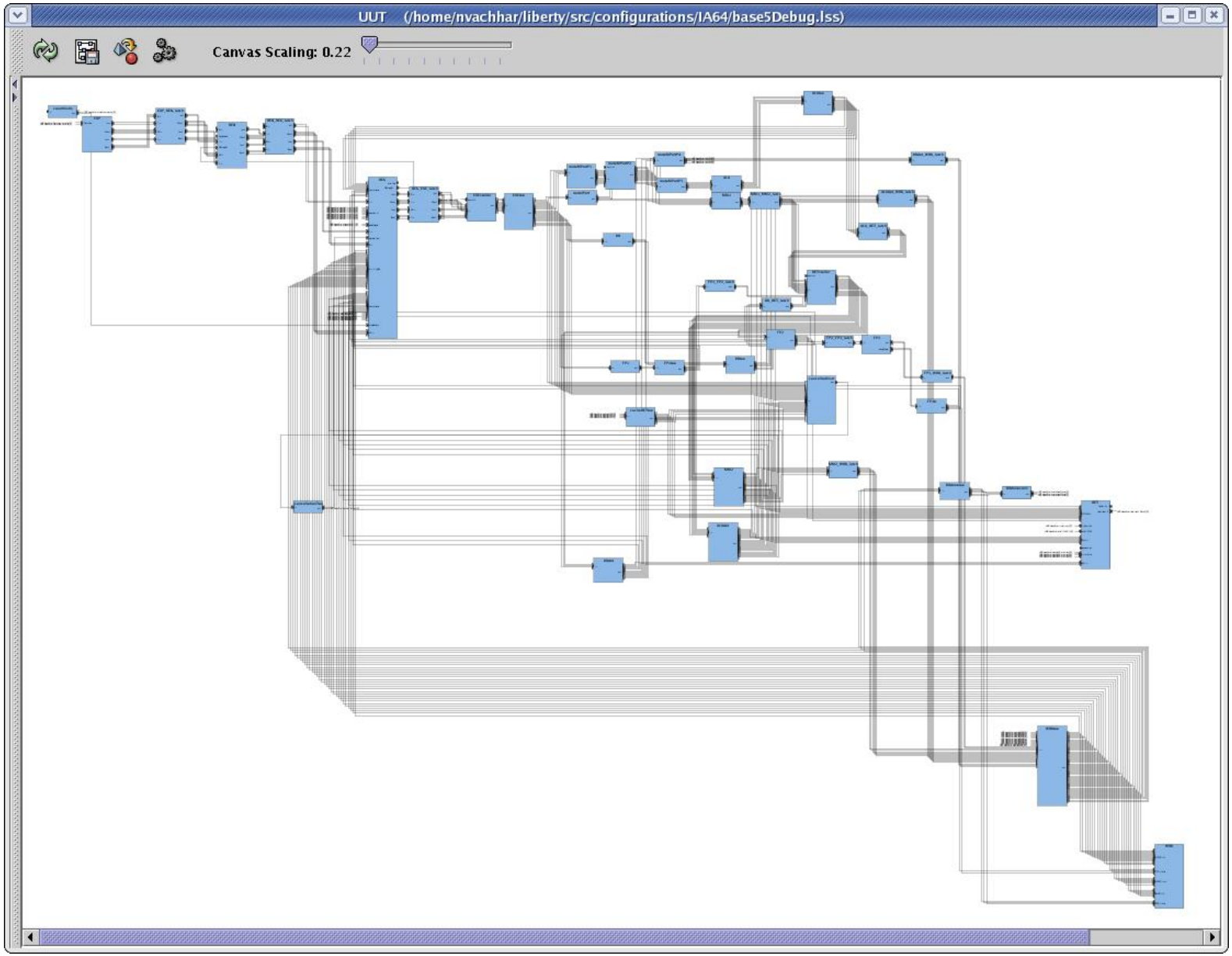
Live Demo
Building a Simple IA64 Processor Model

Demo Details

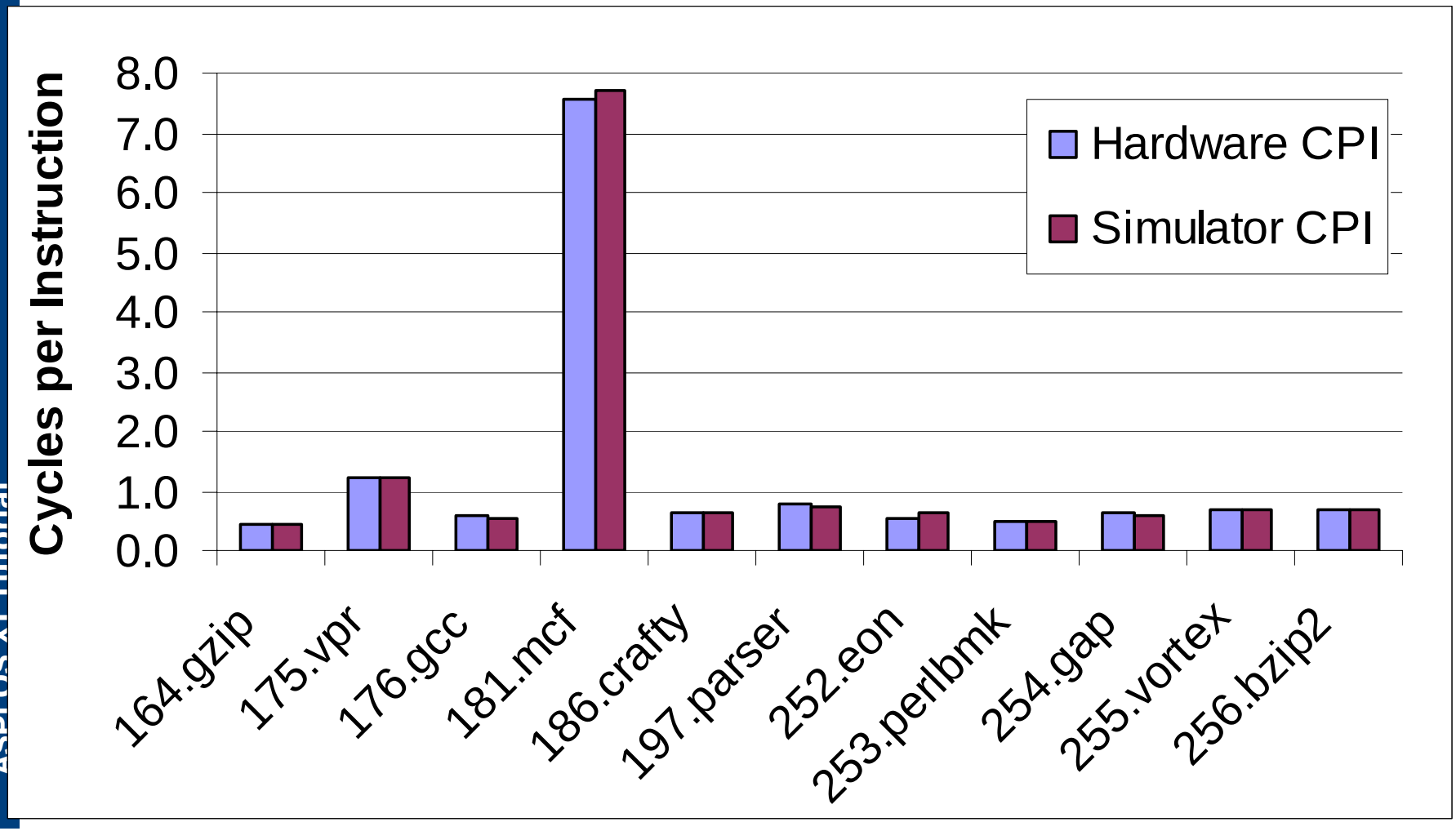


- IA64 Emulator w/ reusable components for μarch
- Port of SimpleScalar Emulator Interface
- Others possible
  - Simics interface, ARM, etc.

Itanium 2 Model



An Itanium 2 Simulator with LSS



- Itanium 2 simulator built using LSS by one person in 11 weeks!
- Average accuracy within 3% of actual hardware

Running OS-level Code

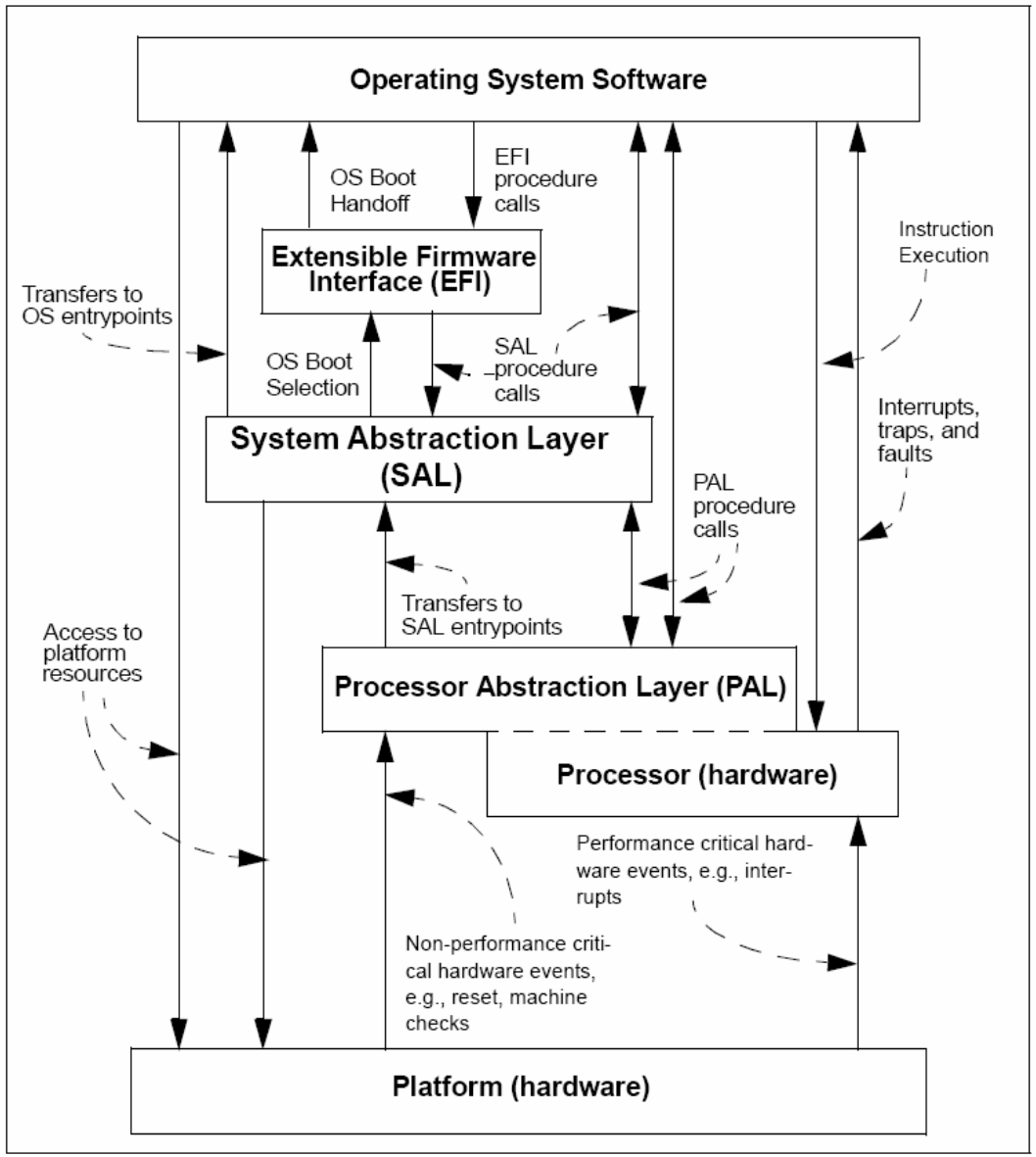
Full System Simulation/Emulation Issues

- Firmware
- Virtual Memory Management
- Interrupt Handling
- Device Support

Firmware Overview

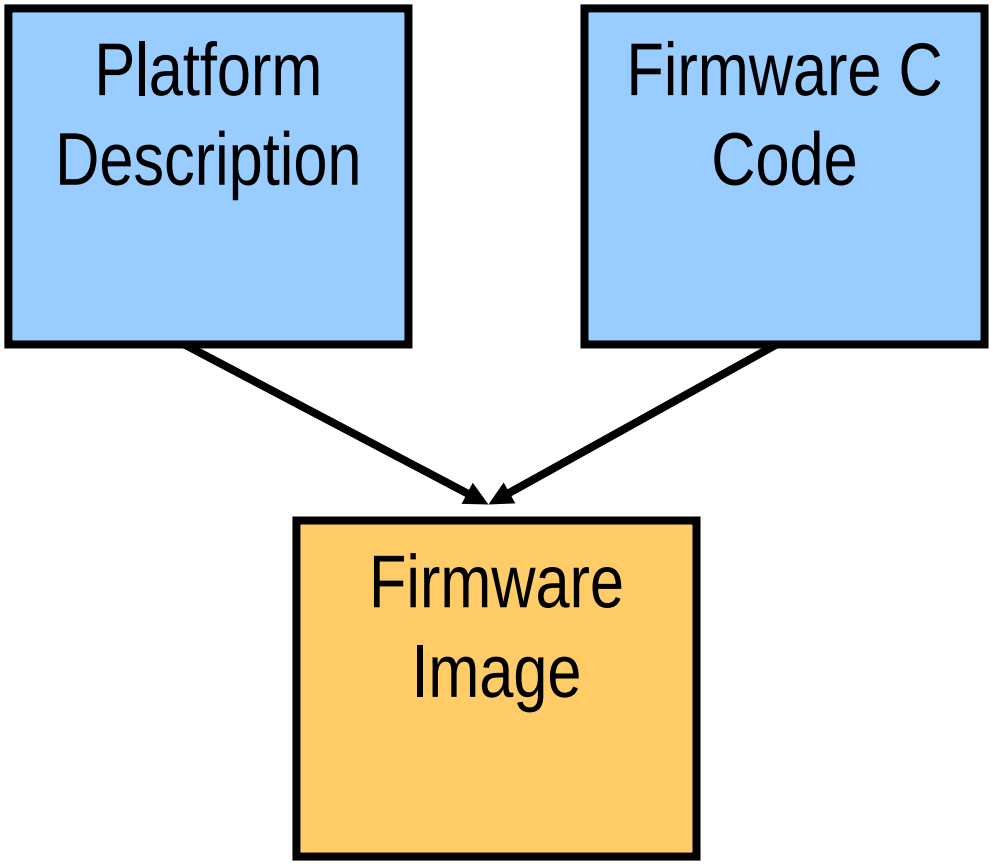
- Processor Abstraction Layer (PAL)
  - Abstracts processor implementation
- System Abstraction Layer (SAL)
  - Abstracts platform implementation
- Extensible Firmware Interface (EFI)
  - Interface between the OS and the platform firmware

Firmware Overview



Intel IA64 Software Developer's Manual Volume 2

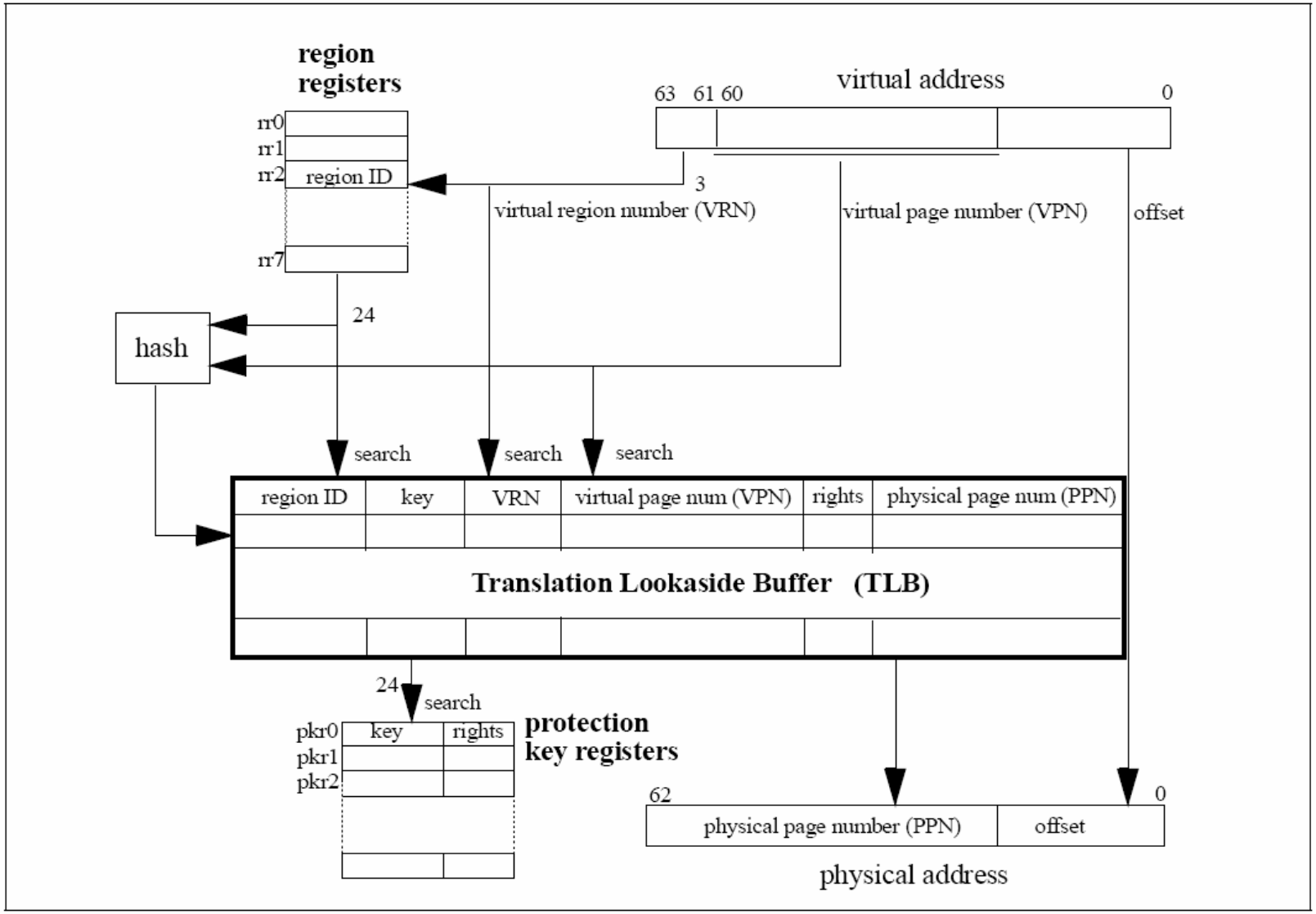
IA64 Emulator Firmware



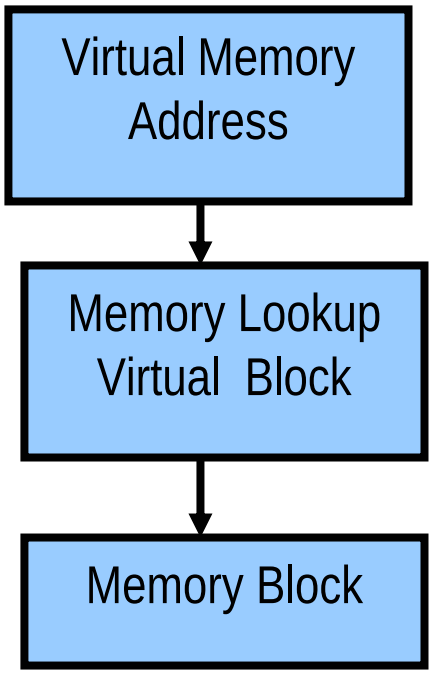
Virtual Memory Management

- Hardware Structures
  - Translation Lookaside Buffer
    - Instruction/Data Translation Registers/Translation Caches
  - Region Registers
    - 8 Region registers can identify up to 2^{24} 61-bit address spaces
  - Protection Key Registers
    - Permit domain-granular protection for page access

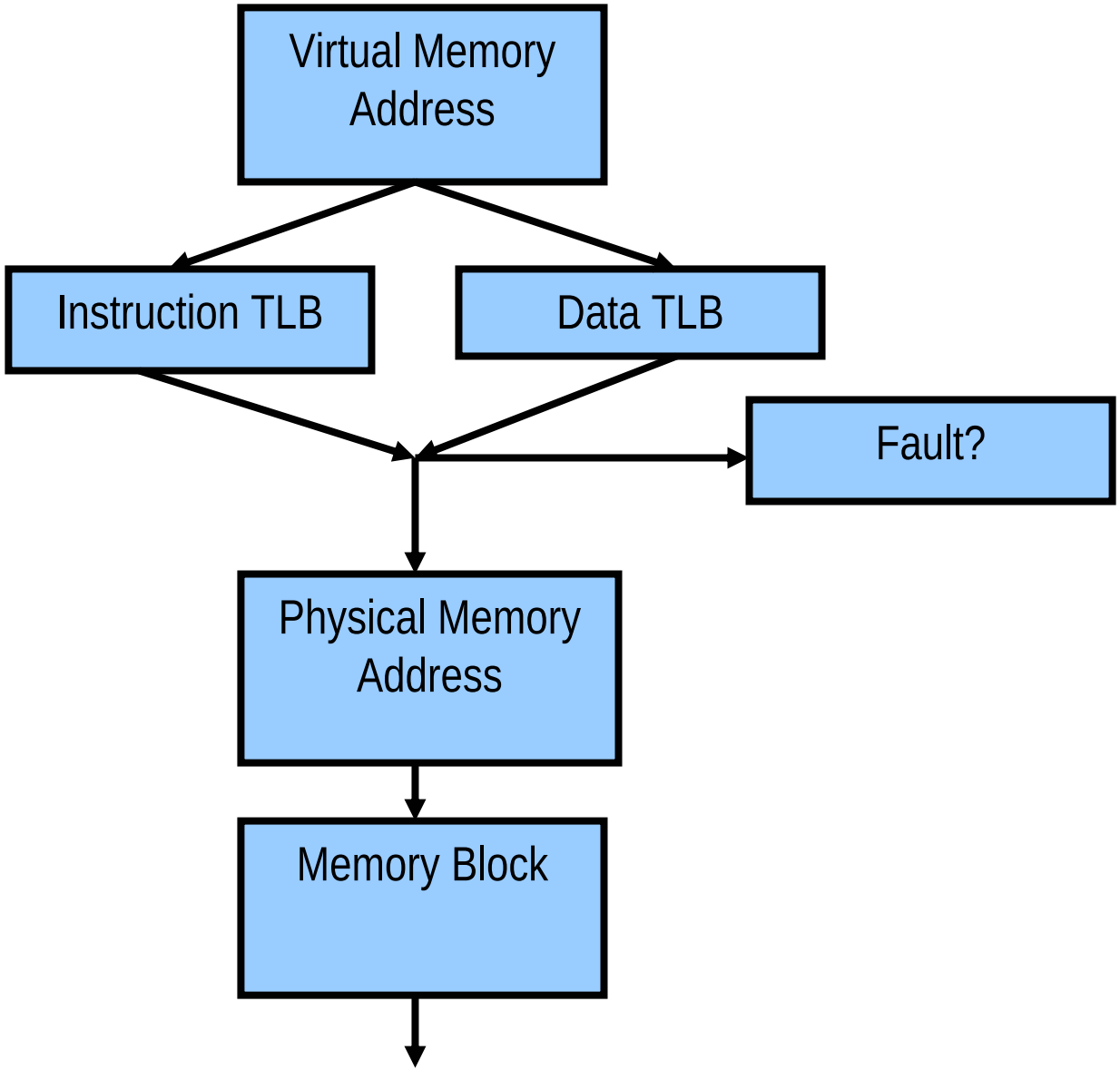
Virtual Memory Management



IA64 Emulator Virtual Memory Management



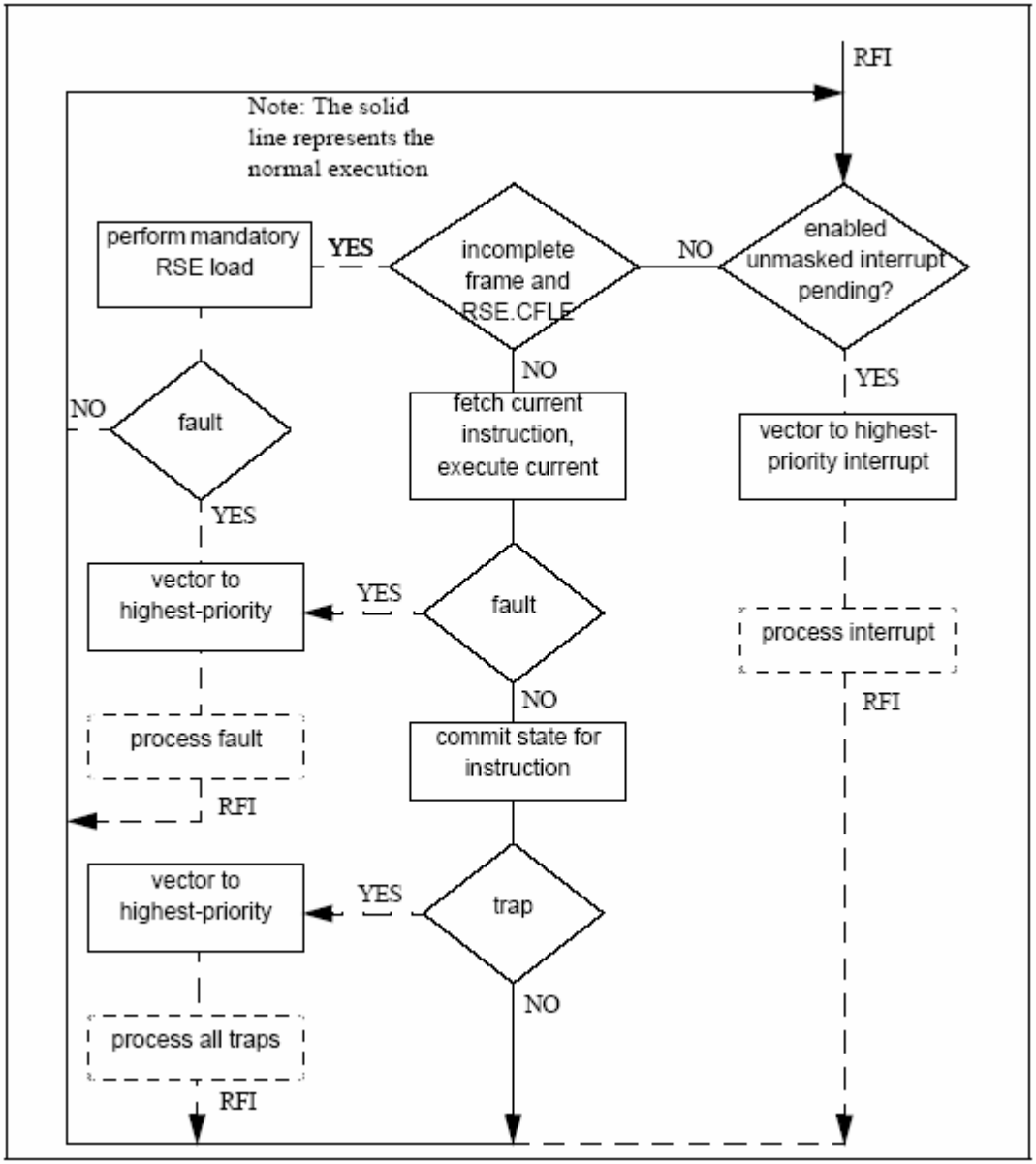
IA64 Emulator Virtual Memory Management



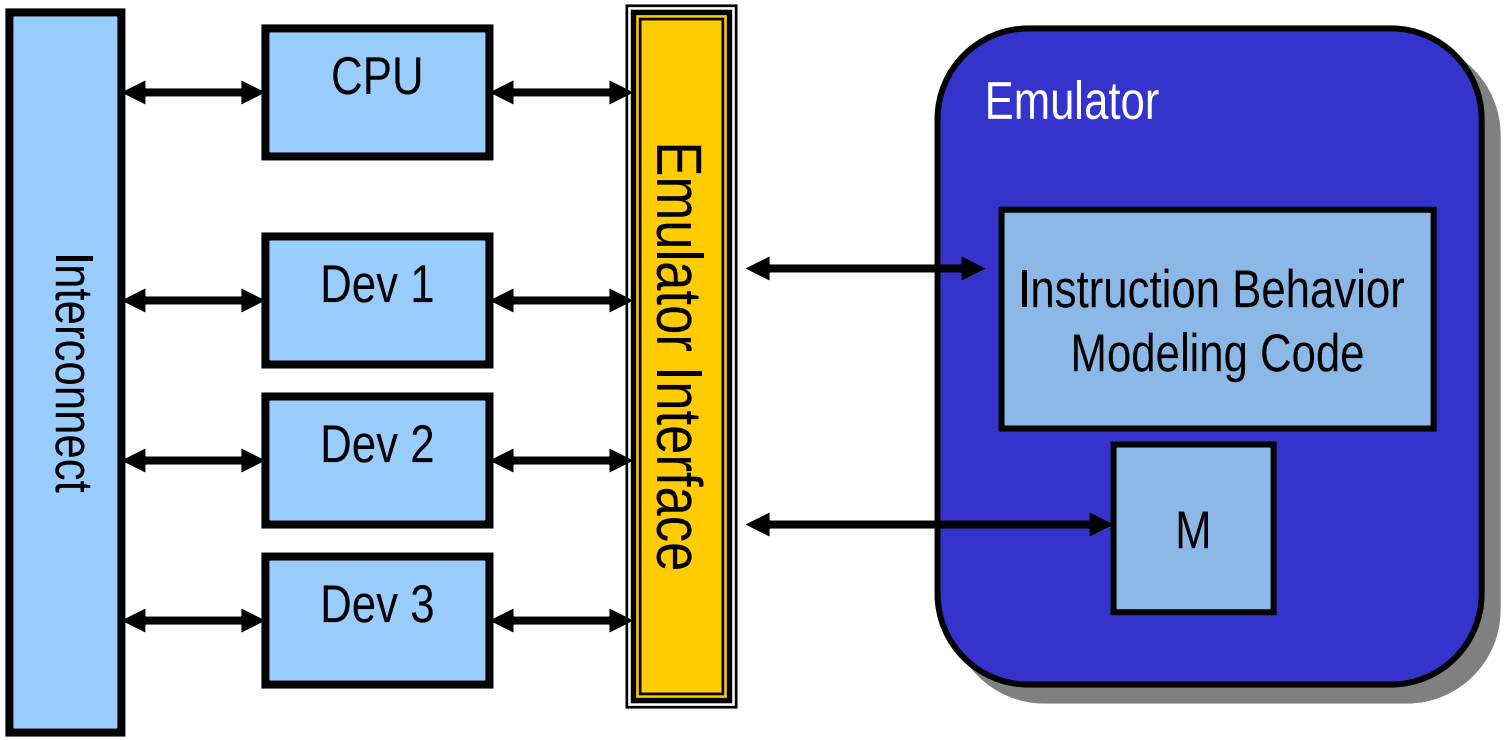
IA64 Interrupt Handling

- IVA-Based: OS serviced interruptions vectored in the interruption vector table
- PAL-Based: Serviced by PAL firmware, system firmware, vectored through hardware entry points directly into PAL firmware
- Interruption Types:
  - Initialization
  - Platform Management
  - External (Non-Maskable/External Controller)

IA64 Interrupt Handling



Adding Device Support to LSE Timing Models



Multiple Clock Domains

- Current release supports single synchronous clock
- Next release of LSE will support multiple clocks

- Instantiate clocks

```
LSE_clock::create("clock1", 100, 0)
LSE_clock::create("clock2", 35, 50)
```

- Assign module instances a clock (or multiple clocks for boundary modules)

- System automatically manages scheduling and time management

End of Talk

Tutorial Sequence

8:00	Welcome	
8:05	LSE Introduction and Philosophy	David
	LSE Basics	Manish
	Your First Configuration	Neil
10:00	Refreshment Break (30 Minutes)	
10:30	Emulators	Manish and Neil
	Building Processor Model	Manish and Neil
	Running OS Code	Jason
	Putting It All Together	David
	The Future of Liberty	David
12:30	Adjourn	

IN CONGRESS, JULY 4, 1776.

The unanimous Declaration of the thirteen united States of America,

When in the Course of human events, it becomes necessary for one people to dissolve the political bands which have connected them with another, and to assume among the powers of the earth, the separate and equal station to which the Laws of Nature and of Nature's God entitle them, a decent respect to the opinions of mankind requires that they should declare the causes which impel them to the separation. ——— We hold these truths to be self-evident, that all men are created equal, that they are endowed by their Creator with certain unalienable Rights, that among these are Life, Liberty and the pursuit of Happiness. — That to secure these rights, Governments are instituted among Men, deriving their just powers from the consent of the governed, — That whenever any Form of Government becomes destructive of these ends, it is the Right of the People to alter or to abolish it, and to institute new Government, laying its foundation on such principles and organizing its powers in such form, as to them shall seem most likely to effect their Safety and Happiness. Prudence, indeed, will dictate that Governments long established should not be changed for light and transient causes; and accordingly all experience hath shewn, that mankind are more disposed to suffer, while evils are sufferable, than to right themselves by abolishing the forms to which they are accustomed. But when a long train of abuses and usurpations, pursuing invariably the same Object evinces a design to reduce them under absolute Despotism, it is their right, it is their duty, to throw off such Government, and to provide new Guards for their future security. — Such has been the patient sufferance of these Colonies; and such is now the necessity which constrains them to alter their former Systems of Government. The history of the present King of Great Britain is a history of repeated injuries and usurpations, all having in direct object the establishment of an absolute Tyranny over these States. To prove this, let Facts be submitted to a candid world. ——— He has refused his Assent to Laws, the most wholesome and necessary for the public good. ——— He has forbidden his Governors to pass Laws of immediate and pressing importance, unless suspended in their operation till his Assent should be obtained; and when so suspended, he has utterly neglected to attend to them. ——— He has refused to pass other Laws for the accommodation of large districts of people, unless those people would relinquish the right of Representation in the Legislature, a right inestimable to them and formidable to tyrants only. ——— He has called together legislative bodies at places unusual, uncomfortable, and distant from the depository of their public Records, for the sole purpose of fatiguing them into compliance with his measures. ——— He has dissolved Representative Houses repeatedly, for opposing with manly firmness his invasions on the rights of the people. ——— He has refused for a long time, after such dissolutions, to cause others to be elected; whereby the Legislative powers, incapable of Annihilation, have returned to the People at large for their exercise; the State remaining in the mean time exposed to all the dangers of invasion from without, and convulsions within. ——— He has endeavored to prevent the population of these States; for that purpose obstructing the Laws for Naturalization of Foreigners; refusing to pass others to encourage their migrations hither, and raising the conditions of new Appropriations of Lands. ——— He has obstructed the Administration of Justice, by refusing his Assent to Laws for establishing Judiciary powers. ——— He has made Judges dependent on his Will alone, for the tenure of their offices, and the amount and payment of their salaries. ——— He has erected a multitude of New Offices, and sent hither swarms of Officers to harass our people, and eat out their substance. ——— He has kept among us, in times of peace, Standing Armies without the Consent of our legislatures. ——— He has affected to render the Military independent of and superior to the Civil power. ——— He has combined with others to subject us to a jurisdiction foreign to our constitution, and unacknowledged by our laws; giving his Assent to their Acts of pretended Legislation: — For Quartering large bodies of armed troops among us: — For protecting them, by a mock Trial, from punishment for any Murders which they should commit on the Inhabitants of these States: — For cutting off our Trade with all parts of the world: — For imposing Taxes on us without our Consent: — For depriving us in many cases, of the benefits of Trial by jury: — For transporting us beyond Seas to be tried for pretended offences. — For abolishing the free System of English Laws in a neighbouring Province, establishing therein an Arbitrary government, and enlarging its Boundaries so as to render it at once an example and fit instrument for introducing the same absolute rule into these Colonies: ——— For taking away our Charters, abolishing our most valuable Laws, and altering fundamentally the Forms of our Governments: — For suspending our own Legislatures, and declaring themselves invested with power to legislate for us in all cases whatsoever. — He has abdicated Government here, by declaring us out of his Protection and waging War against us. ——— He has plundered our seas, ravaged our Coasts, burnt our towns, and destroyed the lives of our people. ——— He is at this time transporting large Armies of foreign Mercenaries to compleat the works of death, desolation and tyranny, already begun with circumstances of Cruelty & Perfidy scarcely paralleled in the most barbarous ages, and totally unworthy the Head of a civilized nation. ——— He has constrained our fellow Citizens taken Captive on the high Seas to bear Arms against their Country, to become the executioners of their friends and Brethren, or to fall themselves by their Hands. — He has excited domestic insurrections amongst us, and has endeavoured to bring on the inhabitants of our frontiers, the merciless Indian Savages, whose known rule of warfare, is an undistinguished destruction of all ages, sexes and conditions. *In every stage of these Oppressions We* have Petitioned for Redress in the most humble terms: Our repeated Petitions have been answered only by repeated injury. A Prince, whose character is thus marked by every act which may define a Tyrant, is unfit to be the ruler of a free people. Nor have We been wanting in attentions to our British brethren. We have warned them from time to time of attempts by their legislature to extend an unwarrantable jurisdiction over us. We have reminded them of the circumstances of our emigration and settlement here. We have appealed to their native justice and magnanimity, and we have conjured them by the ties of our common kindred to disavow these usurpations, which, would inevitably interrupt our connections and correspondence. They too have been deaf to the voice of justice and of consanguinity. We must, therefore, acquiesce in the necessity, which denounces our Separation, and hold them, as we hold the rest of mankind, Enemies in War, in Peace Friends. ———

We, therefore, the Representatives of the united States of America, in General Congress, Assembled, appealing to the Supreme Judge of the world for the rectitude of our intentions, do, in the Name, and by authority of the good People of these Colonies, solemnly publish and declare, That these United Colonies are, and of Right ought to be **Free and Independent States**; that they are Absolved from all Allegiance to the British Crown, and that all political connection between them and the State of Great Britain, is and ought to be totally dissolved; and that as Free and Independent States, they have full Power to levy War, conclude Peace, contract Alliances, establish Commerce, and to do all other Acts and Things which Independent States may of right do. ——— And for the support of this Declaration, with a firm reliance on the protection of divine Providence, we mutually pledge to each other our Lives, our Fortunes and our sacred Honor.

John Hancock

Josiah Bartlett
Wm Whipple
Sam Adams

Button Gwinnett
Lyman Hall
Geo Walton

Wm Hooper
Joseph Hewes
John Penn

Robt Morris
Benjamin Rush
Benj Franklin
John Morton
Geo Clymer
Jas Smith
Geo Taylor
James Wilson
Geo Ross

Wm Floyd
Phil Livingston
Fran Lewis
Lewis Morris

John Adams
Robt Treat Paine
Elbridge Gerry

Step Hopkins
William Ellery

Roger Sherman
Sam Huntington
Wm Williams
Oliver Wolcott

Edward Rutledge
Thos Heyward Junr
Thomas Lynch Junr
Arthur Middleton

Samuel Chase
Wm Paca
Thos Stone
Chas Carroll of Carrollton

George Wythe
Richard Henry Lee
Th Jefferson
Benj Harrison
Thos Nelson Jr
Francis Lightfoot Lee
Carter Braxton

Wm Paca
Geo Read
Thos M:Kean

Casar Rodney
Geo Read
Tho M:Kean

Wm Duer
Lewis Morris

Wm Whipple
Matthew Thornton

Abra Clark

Tutorial Sequence

8:00	Welcome	
8:05	LSE Introduction and Philosophy	David
	LSE Basics	Manish
	Your First Configuration	Neil
10:00	Refreshment Break (30 Minutes)	
10:30	Emulators	Manish and Neil
	Building Processor Model	Manish and Neil
	Running OS Code	Jason
	Putting It All Together	David
	The Future of Liberty	David
12:30	Adjourn	

Now It Is Your Turn

- We did lots of research to get structural modeling right
- Many have benefited greatly from this powerful reuse

- LSE has become a standard framework for the exchange of architectural components and designs

- The power of this reuse is related to the number of users in the community, so...

Join In!

The Free Spirit

In this vein, we strive to grow this community...

LSE tools and libraries are non-copylefted free software

- Share your ideas with companies
- Use LSE in your company

We respond to your feedback

- Let us know what features you would like
- Tell us about your likes/dislikes

Stay in Touch

Mailing Lists

See Liberty Website To Sign Up

liberty@lists.cs.princeton.edu:

- Liberty Research Group Announcements - very low traffic

liberty-lse-install@lists.cs.princeton.edu:

- Installation Issues and Questions

liberty-lse-users@lists.cs.princeton.edu:

- User community
  - Share modules/configs with others - exploit reuse...
  - Initiate collaborations with others - exploit reuse...
- Watch here for LSE updates, new tools
- Usage support

What to do Next?

Try LSE!

You have the CD and *Getting Started with LSE*

1. Install LSE
2. Read the documentation (we have lots!!)
   - Getting Started with LSE
   - The LSE Core Module Library Reference
   - The LSE User's Manual
   - The LSE Visualizer Manual
   - The LSE API Reference Manual
   - The LSE Developer's Manual
   - The LSE Internals Manual

What to do Next?

Try LSE!

You have the CD and *Getting Started with LSE*

1. Install LSE
2. Read the documentation (we have lots!!)
3. Play with sample configurations, emulators
   - LFSR
   - Tomasulo DLX
   - IA-64

What to do Next?

Try LSE!

You have the CD and *Getting Started with LSE*

1. Install LSE
2. Read the documentation (we have lots!!)
3. Play with sample configurations, emulators
4. Use LSE in your research/development
5. Keep in touch (visit us!)
6. Check the website for updates

Motivation for Future Tools Work

The Future Liberty Tool Collection

Application(s)

Auto-Explorer

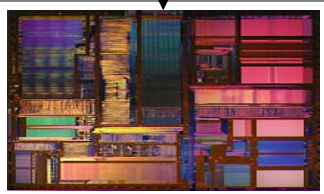
The VELOCITY Compiler

LSS+GLAD

LSE

Optimized Executables

Architectural Simulator Instance



Shameless Research Plug

The Liberty Research Group

- Remove human intervention from the “critical path”
- Understanding and designing for compiler and architectural optimization interactions
  - Redefine the hardware/software interface
  - “How to do” not just “what to do”
  - Far ILP
- Question the artificial boundaries present in compilers
  - Liberate us from inlining once and for all!
  - Phase order/optimization issues
- Reliability guarantees

Thank you!

- We are very excited about the future for LSE
- Thank you for joining us today

END OF TUTORIAL

The Liberty Research Group
Princeton University